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MAXIM INTEGRATED PRODUCTS, INC.

UNITED STATES DISTRICT COURT

NORTHERN DISTRICT OF CALIFORNIA

SAN FRANCISCO DIVISION

MAXIM INTEGRATED PRODUCTS, INC., Plaintiff, v. FREESCALE SEMICONDUCTOR, INC., Defendant.	Case No. CV 08-00979-MHP **AMENDED COMPLAINT FOR DECLARATORY JUDGMENT AND DEMAND FOR JURY TRIAL**

Pursuant to the parties' agreement to narrow the scope of the present dispute, filed with the Court on April 28, 2008, Plaintiff Maxim Integrated Products, Inc. ("Maxim"), for its Amended Complaint against Defendant Freescale Semiconductor, Inc. ("Freescale"), avers as follows:

PARTIES

1. Plaintiff Maxim is a corporation organized and existing under the laws of the state of Delaware, with its principal place of business at 120 San Gabriel Drive, Sunnyvale, California 94086.

2. On information and belief, Defendant Freescale is a corporation organized and existing under the laws of Delaware, with its principal place of business at 6501 William Cannon Drive West, Austin, Texas 78735, which does business in this District and elsewhere in the State of California.

JURISDICTION AND VENUE

3. This action seeks a declaratory judgment under the Declaratory Judgment Act, 28 U.S.C. §§2201 and 2202. It presents an actual case or controversy under Article III of the United States Constitution and serves a useful purpose in clarifying and settling the legal rights at issue.

4. Freescale claims to own the following patents (collectively, "the Freescale patents"):

U.S. Patent No. 5,089,722 ("the '722 patent") entitled "High speed output buffer circuit with overlap current control," a true and correct copy of which is attached as Exhibit A,

U.S. Patent No. 5,105,250 ("the '250 patent") entitled "Heterojunction bipolar transistor with a thin silicon emitter," a true and correct copy of which is attached as Exhibit B,

U.S. Patent No. 5,172,214 ("the '214 patent") entitled "Leadless semiconductor device and method for making the same," a true and correct copy of which is attached as Exhibit C,

U.S. Patent No. 5,200,362 ("the '362 patent") entitled "Method of attaching conductive traces to an encapsulated semiconductor die using a removable transfer film," a true and correct copy of which is attached as Exhibit D,

U.S. Patent No. 5,434,739 ("the '739 patent") entitled "Reverse battery protection circuit," a true and correct copy of which is attached as Exhibit E,

U.S. Patent No. 5,476,816 ("the '816 patent") entitled "Process for etching an insulating layer after a metal etching step," a true and correct copy of which is attached as Exhibit F, and

U.S. Patent No. 5,776,798 ("the '798 patent") entitled Semiconductor package and method thereof," a true and correct copy of which is attached as Exhibit G.

5. Maxim seeks a judgment against Freescale that the accused Maxim products and processes have not infringed and do not infringe the asserted claims of the Freescale patents and/or that these claims are invalid and/or unenforceable.

6. This Court has subject matter jurisdiction over this action under 28 U.S.C. §§ 1331 and 1338(a) because the action arises under the patent laws of the United States, 35 U.S.C. §1 et seq.

7. Venue in this district is proper pursuant to 28 U.S.C. §§ 1391(b) and (c).

INTRADISTRICT ASSIGNMENT

8. This action is an intellectual property case and pursuant to Civil L.R. 3.2(c), it should be assigned on a districtwide basis.

GENERAL ALLEGATIONS

9. Maxim manufactures and sells various semiconductor devices or integrated circuits.

10. On November 16, 2005, Freescale provided a book of patent claim charts to Maxim alleging that Maxim and/or Maxim devices infringe various patents, including the '722 patent, the '250 patent, the '739 patent, the '816 patent, and the '798 patent ("the first set of Freescale patents").

11. In a subsequent letter dated July 14, 2006, Freescale specifically stated its claim charts previously provided for the first set of Freescale patents "provide notice to Maxim regarding infringement of [the first set of] Freescale patents by Maxim products." With this letter, Freescale also provided ten new claim charts, including charts for the '214 patent and the '362 patent ("the second set of Freescale patents"), which Freescale alleged "provide notice of [] new patents to Maxim, and identify new Maxim products."

12. Freescale asserts that Maxim infringes the Freescale patents and needs a license to these patents, but Maxim disagrees. Maxim and Freescale met via conference call on August 8, 2007, November 30, 2007, and January 7, 2008, and in person on February 15,

2008, in an attempt to resolve the dispute.

13. Maxim and Freescale have been unable to reach any agreement with respect to Freescale's patent infringement allegations. Those discussions are now at an impasse.

14. Maxim is not liable for infringing any asserted claim of the Freescale patents because each such claim is invalid, the accused Maxim products and processes have not infringed any such valid claim, and/or the asserted claims are unenforceable.

15. Accordingly, there is an actual, substantial and continuing justiciable controversy between Maxim and Freescale regarding the validity and enforceability of the Freescale patents and regarding alleged infringement of the Freescale patents by Maxim or by use of Maxim's products and processes.

FIRST CLAIM FOR RELIEF

Declaratory Relief — the '722 Patent

16. Maxim incorporates by reference each and every allegation set forth in paragraphs 1-15 of the Complaint.

17. Maxim seeks and is entitled to a declaration that its accused products and/or processes do not directly or indirectly infringe any asserted claim of the '722 patent and/or that each such claim is invalid and/or unenforceable for failure to meet one or more of the conditions of patentability set forth in §§ 101, 102, 103 and 112 of Title 35 of the United States Code.

SECOND CLAIM FOR RELIEF

Declaratory Relief — the '250 Patent

18. Maxim incorporates by reference each and every allegation set forth in paragraphs 1-17 of the Complaint.

19. Maxim seeks and is entitled to a declaration that its accused products and/or processes do not directly or indirectly infringe any asserted claim of the '250 patent and/or that each such claim is invalid and/or unenforceable for failure to meet one or more of the conditions of patentability set forth in §§ 101, 102, 103 and 112 of Title 35 of the United States Code.

THIRD CLAIM FOR RELIEF

Declaratory Relief — the '214 Patent

20. Maxim incorporates by reference each and every allegation set forth in paragraphs 1-19 of the Complaint.

21. Maxim seeks and is entitled to a declaration that its accused products and/or processes do not directly or indirectly infringe any asserted claim of the '214 patent and/or that each such claim is invalid and/or unenforceable for failure to meet one or more of the conditions of patentability set forth in §§ 101, 102, 103 and 112 of Title 35 of the United States Code.

FOURTH CLAIM FOR RELIEF

Declaratory Relief — the '362 Patent

22. Maxim incorporates by reference each and every allegation set forth in paragraphs 1-21 of the Complaint.

23. Maxim seeks and is entitled to a declaration that its accused products and/or processes do not directly or indirectly infringe any asserted claim of the '362 patent and/or that each such claim is invalid and/or unenforceable for failure to meet one or more of the conditions of patentability set forth in §§ 101, 102, 103 and 112 of Title 35 of the United States Code.

FIFTH CLAIM FOR RELIEF

Declaratory Relief — the '739 Patent

24. Maxim incorporates by reference each and every allegation set forth in paragraphs 1-23 of the Complaint.

25. Maxim seeks and is entitled to a declaration that its accused products and/or processes do not directly or indirectly infringe any asserted claim of the '739 patent and/or that each such claim is invalid and/or unenforceable for failure to meet one or more of the conditions of patentability set forth in §§ 101, 102, 103 and 112 of Title 35 of the United States Code.

SIXTH CLAIM FOR RELIEF

Declaratory Relief — the '816 Patent

26. Maxim incorporates by reference each and every allegation set forth in paragraphs 1-25 of the Complaint.

27. Maxim seeks and is entitled to a declaration that its accused products and/or processes do not directly or indirectly infringe any asserted claim of the '816 patent and/or that each such claim is invalid and/or unenforceable for failure to meet one or more of the conditions of patentability set forth in §§ 101, 102, 103 and 112 of Title 35 of the United States Code.

SEVENTH CLAIM FOR RELIEF

Declaratory Relief — the '798 Patent

28. Maxim incorporates by reference each and every allegation set forth in paragraphs 1-27 of the Complaint.

29. Maxim seeks and is entitled to a declaration that its accused products and/or processes do not directly or indirectly infringe any asserted claim of the '798 patent and/or that each such claim is invalid and/or unenforceable for failure to meet one or more of the conditions of patentability set forth in §§ 101, 102, 103 and 112 of Title 35 of the United States Code.

PRAYER FOR RELIEF

Wherefore, Maxim prays for relief as follows:

1. On Maxim's First through Seventh Claims for Relief:

(a) For a declaratory judgment that Maxim's accused products and processes do not infringe, contributorily infringe or induce infringement of, and have never infringed, contributorily infringed or induced infringement of, one or more claims of the Freescale patents;

(b) For a declaratory judgment that one or more claims of the Freescale Patents are invalid and/or that one or more of the Freescale Patents are unenforceable;

(c) For the Court to declare this to be an exceptional case within the meaning of

35 U.S.C. § 285, entitling Maxim to an award of its reasonable attorneys' fees in this action;

(d) For an award to Maxim of all costs and expenses of this action; and

(d) For such other and further relief as the Court may deem just and proper.

April 30, 2008

Respectfully submitted,

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JO DALE CAROTHERS (BAR NO. 228703)

Attorneys for Plaintiff
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DEMAND FOR JURY TRIAL

Plaintiff Maxim demands a jury trial on all issues triable of right by jury.

April 30, 2008

Respectfully submitted,

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LAURA E. UNDERWOOD-MUSCHAMP (BAR NO. 228717)
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CERTIFICATE OF SERVICE

I hereby certify that all counsel of record, who are deemed to have consented to electronic service are being served this 30th day of April 2008, with a copy of this document via the Court's CM/ECF system. Any other counsel of record will be served by electronic mail on this same date.

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EXHIBIT A

US005089722A

United States Patent [19]

Amedeo

[11] Patent Number: 5,089,722

[45] Date of Patent: Feb. 18, 1992

[54] **HIGH SPEED OUTPUT BUFFER CIRCUIT WITH OVERLAP CURRENT CONTROL**

[75] Inventor: **Robert J. Amedeo**, Austin, Tex.

[73] Assignee: **Motorola, Inc.**, Schaumburg, Ill.

[21] Appl. No.: **503,012**

[22] Filed: **Apr. 2, 1990**

[51] **Int. Cl.**[5] **H03K 17/16**; H03K 19/094; H03K 5/12; H03K 17/687

[52] **U.S. Cl.** **307/443**; 307/451; 307/542; 307/475; 307/548; 307/558; 307/263

[58] **Field of Search** 307/270, 443, 542, 572, 307/448, 451, 452, 585, 552, 555, 558, 568, 592, 594, 597, 246, 263, 242, 475, 547, 548

[56] **References Cited**

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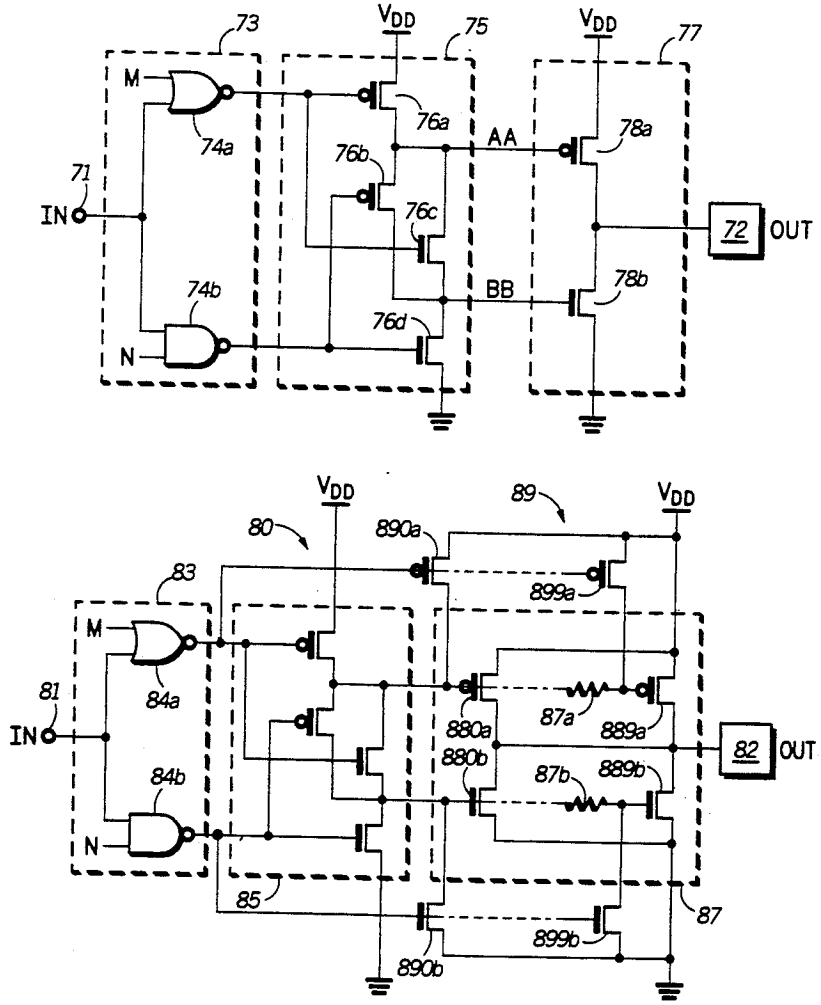
Primary Examiner—Edward P. Westin
Assistant Examiner—David R. Bertelson
Attorney, Agent, or Firm—Robert L. King

[57] **ABSTRACT**

A pre-driver stage includes two pairs of series-stacked transistors for responding to input stage outputs and provides first and second outputs to an output driver stage. The first output becomes low at a certain delay period after the second output becomes low, and the second output becomes high at a certain delay period after the first output becomes high. Therefore, the turn-off of the active driver transistor is completed before the turn-on of the opposite output transistor, inhibiting an overlap current. In another form, the buffer circuit also uses assist transistors placed near the driver transistors for assisting the oppsoite driver transistors in turning off.

14 Claims, 4 Drawing Sheets



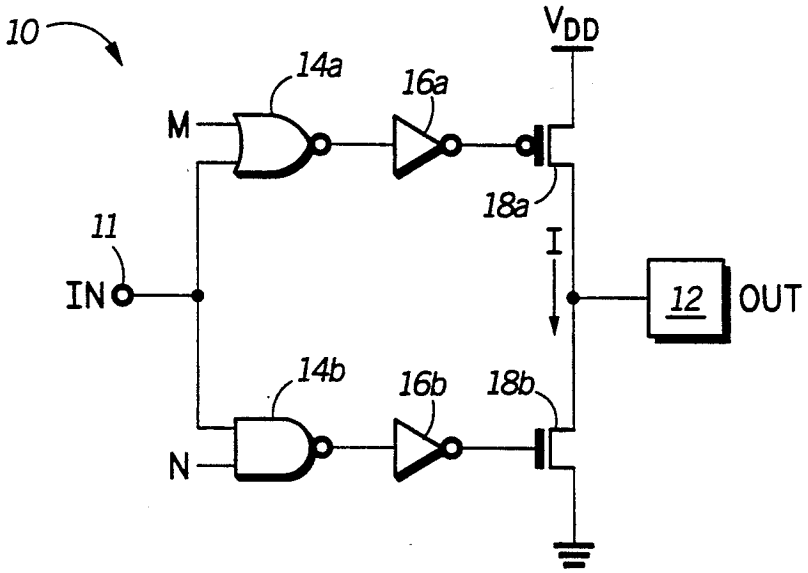


FIG. 1A
-PRIOR ART-

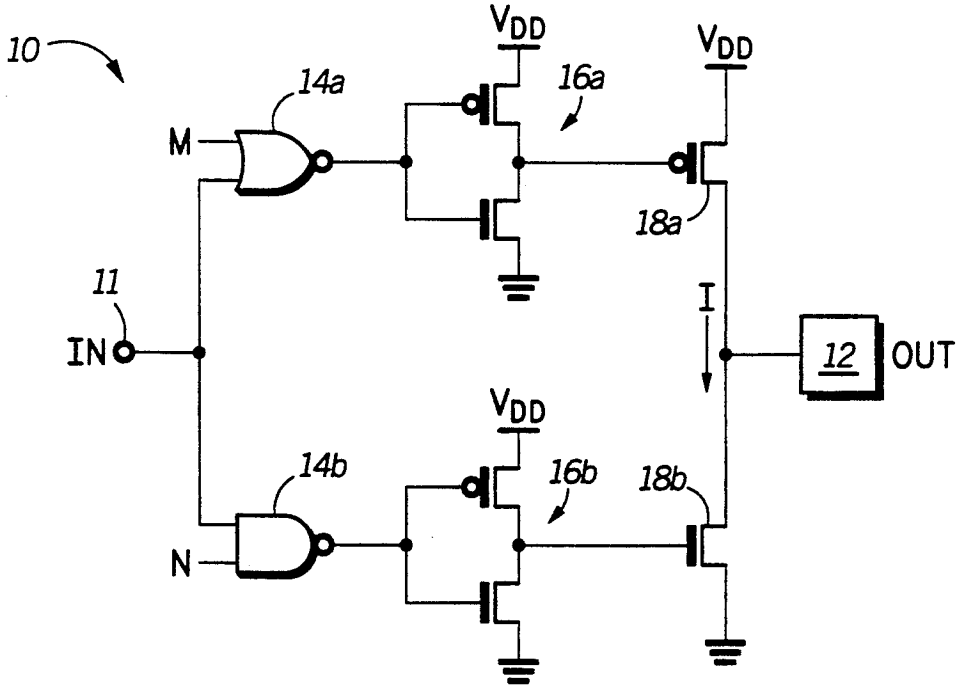


FIG. 1B
-PRIOR ART-

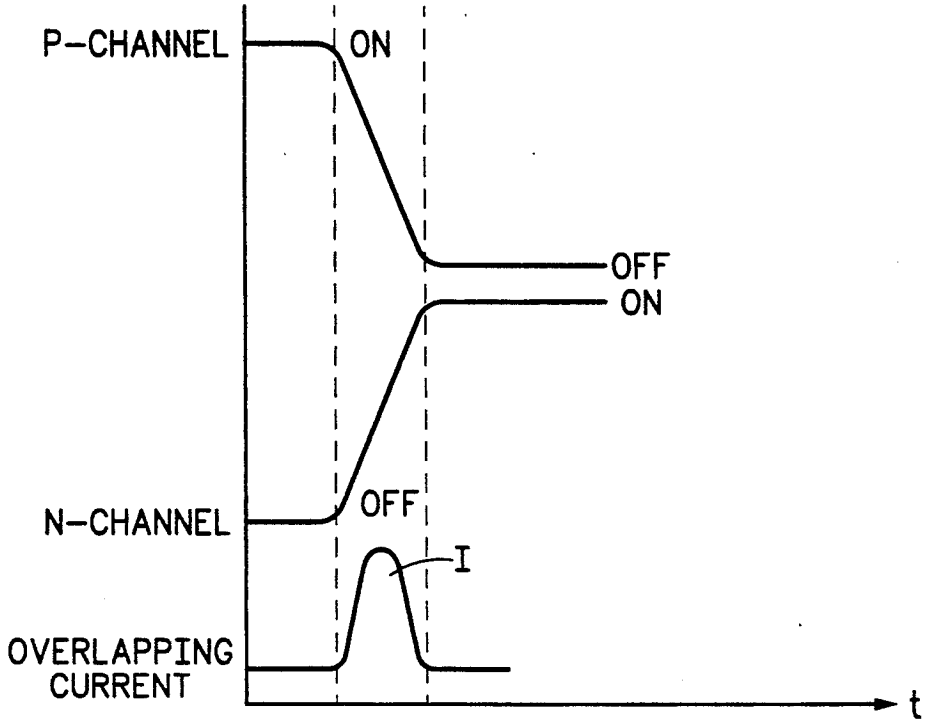


FIG.2

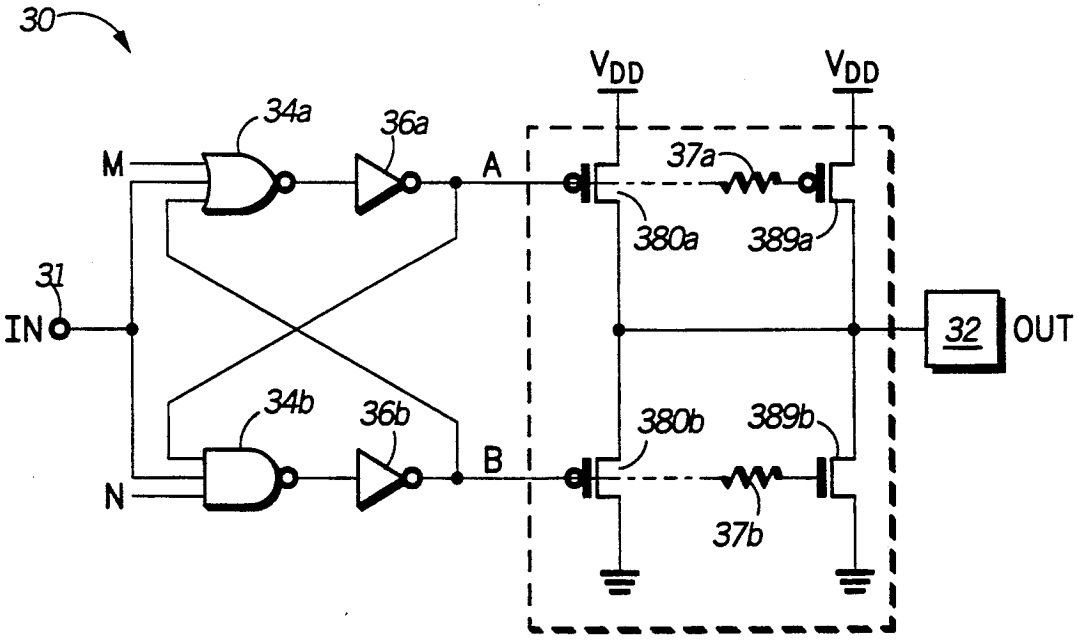


FIG.3
-PRIOR ART-

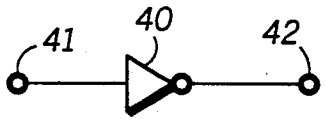


FIG.4A

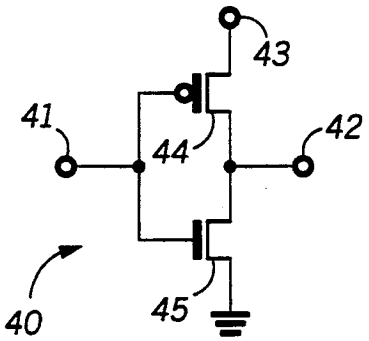


FIG.4B

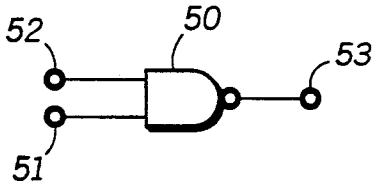


FIG.5A

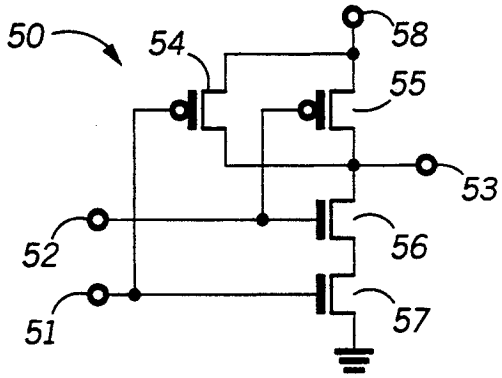


FIG.5B

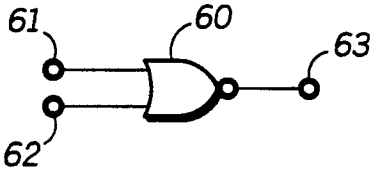


FIG.6A

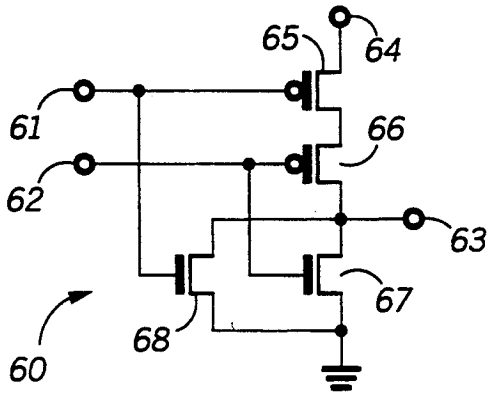
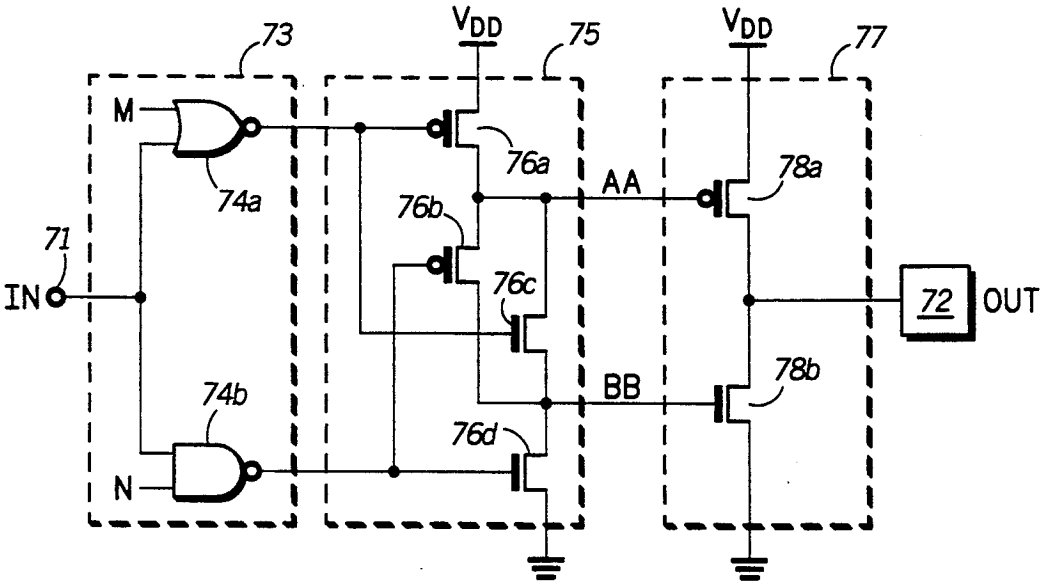


FIG.6B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V_{DD}
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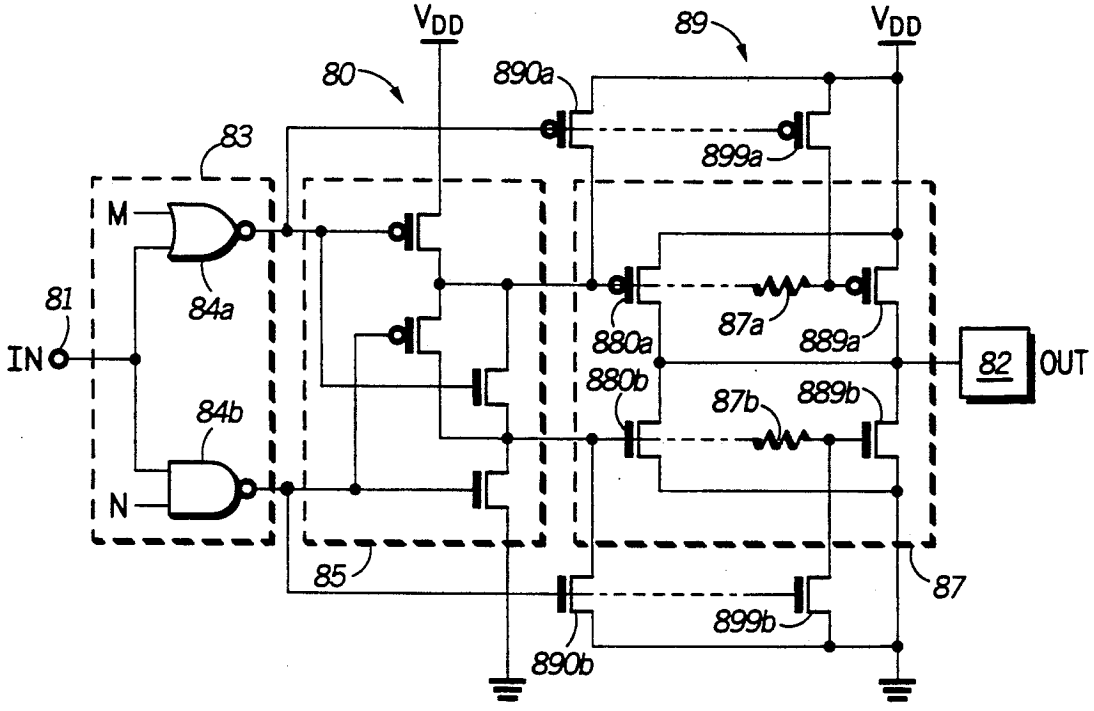
74b
BB
78b
76d
N

FIG. 7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87b
889b
84b
N
85
87
899b
890b

FIG. 8

HIGH SPEED OUTPUT BUFFER CIRCUIT WITH OVERLAP CURRENT CONTROL

FIELD OF THE INVENTION

The present invention relates, in general, to an output buffer circuit. More particularly, the invention relates to a CMOS (complementary metal-oxide-silicon) output buffer circuit with high speed switching and large power handling capacity.

BACKGROUND OF THE INVENTION

Many digital output or driver circuits have been developed for use in MOS FET(field effect transistor) integrated circuitry, especially for use at output pads (terminals) of microprocessors or microcomputers. A CMOS output buffer having a complementary pair of transistors in an output stage is widely used and operates at a relatively high speed and reduces the internal power consumption when the buffer is in one or the other of its two logic states. However, the basic CMOS output buffer has a disadvantage that an overlapping current passes through the P-channel and N-channel transistor of the output stage in the buffer when it is switching from one logic state to the other.

In addition, it is desirable that the conventional buffer circuit be able to source (and sink) a large amount of current to (and from) external circuitry connected thereto. But, it is difficult to drive external large circuit loads by the conventional CMOS output buffer.

Attempts to overcome such defects of the single transistor pair CMOS output buffer include cross-coupling pre-drivers with input logic gates to provide propagation delays. Others have also connected multiple complementary transistor pairs in parallel in an output stage to increase the source and sink currents. However, such cross-coupling buffer circuits require additional interconnections which undesirably increase the complexity of the circuit, and the propagation delay period of the circuit cannot be controlled. Further, the multiple complementary transistor pair output buffer worsens the overlapping current problem, as described below in detail.

SUMMARY OF THE INVENTION

Accordingly, it is an object of the present invention to provide an improved output buffer circuit which has high switching speed with overlap current control.

More particularly, it is an object of the present invention to provide an improved output buffer circuit having large power driving capacity with overlap current control.

Yet another object of the present invention is to provide an improved output buffer circuit which can be easily implemented into existing circuits without additional process steps or area.

In carrying out the above and other objects of the invention there is provided, in one form, an output buffer circuit having a data input terminal for receiving a data signal, and an output signal terminal for providing an output signal. The output buffer circuit comprises an input stage, a pre-driver stage, and an output driver stage having a pair of driver transistors connected in series. The pre-driver stage includes two pairs of stacked transistors for responding to the input stage outputs and provides first and second outputs to the output driver stage. The first output assumes a first logic state after a first predetermined controlled delay period after the second output assumes the first logic state, and the second output assumes a second logic state after a second predetermined controlled delay period after the first output assumes the second logic state. The turn-off of an active driver transistor in the driver stage is completed before the turn-on of a second driver transistor in the driver state, thereby preventing an overlap current.

According to another feature of the invention, the output buffer circuit further comprises assist semiconductor devices placed near the corresponding driver transistors for assisting the driver transistors in turning off.

These and other objects, features, and advantages, will be more clearly understood from the detailed description below together with the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. **1A** is a partial schematic diagram of a known output buffer circuit having a basic CMOS driver;

FIG. **1B** shows the circuit of FIG. **1A**, illustrating the inverters schematically;

FIG. **2** is a graph illustrating the generation of an overlap current in an output driver;

FIG. **3** is a partial schematic diagram of another known output buffer circuit having a cross-coupling structure;

FIGS. **4A** and **4B** show, respectively, the symbol of an inverter and its schematic diagram when implemented utilizing MOS transistors;

FIGS. **5A** and **5B** show, respectively, the symbol for a NAND gate and its schematic diagram utilizing MOS transistors;

FIGS. **6A** and **6B** show, respectively, the symbol for a NOR gate and its schematic diagram utilizing MOS transistors;

FIG. **7** is a schematic diagram of one embodiment of an output buffer circuit of this invention; and

FIG. **8** is a schematic diagram of another embodiment of an output buffer circuit of this invention.

DETAILED DESCRIPTION OF THE INVENTION

As mentioned before, although a conventional basic CMOS output buffer has the advantage of low quiescent current, it also has a disadvantage of an overlap current when switching between logic states. First, a brief reference will be made to a basic CMOS output buffer.

FIG. **1A** schematically shows an example of a known CMOS output buffer. As shown in FIG. **1A**, a basic output buffer circuit **10** includes a data input terminal **11** for receiving a data logic signal IN, and an output signal terminal **12** for providing an output logic signal OUT to external circuitry (not shown). When buffer **10** is receiving a logically high signal at terminal **11**, the logic high signal is applied to a first input of a NOR gate **14***a*, thereby causing NOR gate **14***a* to provide a logic low signal on its output lead which is connected to the input of an inverter **16***a*. The logic state of an enable signal M connected to a second input of NOR gate **14***a* is assumed to be a logic low. Inverter **16***a* supplies at an output a logic high output signal which is applied to the gate of a P-channel MOS (metal-oxide-silicon) FET (field effect transistor) **18***a*, thus making P-channel transistor **18***a* nonconductive.

Simultaneously, the logic high signal at input terminal **11** is applied also to a first input of a NAND gate **14***b* with a second input receiving a logic high enable signal N, thereby causing NAND gate **14***b* to provide a logic low signal at its output which is connected to the input of an inverter **16***b*. Inverter **16***b* supplies on its output a logic high output signal which is applied to the gate of an N-channel MOS transistor **18***b*, thus making N-channel transistor **18***b* conductive.

In this way, with buffer **10** receiving a logic high data signal, P-channel transistor **18***a* is off (nonconductive) and N-channel transistor **18***b* is on (conductive), thus effectively connecting output signal terminal **12** to ground through N-channel transistor **18***b* and disconnecting output signal terminal **12** from the positive supply voltage V_{DD}. Therefore, a logic low output signal is provided and buffer **10** is allowed to sink current from external circuitry (not shown) connected to terminal **12**.

Conversely, when buffer **10** is receiving a logic low input signal, the logic low input signal is applied to the first input of NOR gate **14***a* with the second input thereof receiving a logic low enable signal M, thereby causing NOR gate **14***a* to provide a logic high signal at its output which is connected to the input of inverter **16***a*. Inverter **16***a* supplies at its output a logic low output signal which in turn is applied to the gate of P-channel transistor **18***a*, thus making P-channel transistor **18***a* conductive.

Simultaneously, the logic low signal at input terminal **11** is applied also to the first input of NAND gate **14***b* with the second input thereof still receiving a logic high enable signal N, thereby causing NAND gate **14***b* to provide a logic high at its output which is connected to the input of inverter **16***b*. Inverter **16***b* supplies at its output logic low output signal which in turn is applied to the gate of N-channel transistor **18***b*, thus making N-channel transistor **18***b* nonconductive.

In this manner, with buffer **10** receiving a logic low data signal, output signal terminal **12** is effectively connected to positive supply voltage V_{DD} and is disconnected from ground, therefore providing a logic high output signal and allowing buffer **10** to source current to external circuitry (not shown).

However, in this basic CMOS output buffer **10**, because each signal from inverters **16***a* and **16***b* respectively arrives at the gates of transistors **18***a* and **18***b* simultaneously, P-channel transistor **18***a* turns off and N-channel transistor **18***b* turns on at the same time, as shown by a graph in FIG. **2**, and vice versa. That is, the period of transient logic state of transistor **18***a* overlaps with the transient period of transistor **18***b*. Therefore, during the transient periods of transistors **18***a* and **18***b*, a current I passes from supply voltage V_{DD} through transistors **18***a* and **18***b* to ground. This overlap current (sometimes called "spike current") is especially high in a large output buffer having high power driving capability. The overlap current I is undesirable because it increases internal current consumption and causes RFI (radio frequency interference) which adversely affects other circuitry.

FIG. **3** shows another example of another known output buffer designed to solve the overlap current problem. As shown in FIG. **3**, a cross-coupled output buffer circuit **30** includes a data input terminal **31** for receiving a digital data input signal IN, and an output signal terminal **32** for providing an output signal OUT to external circuitry (not shown). Output buffer **30** also includes a predetermined number of pairs of P-and N-channel MOS transistors **380***a, b* through **389***a, b* as noted by the dashed lines. Input terminal **31** is connected to a first input of a NOR gate **34***a* and to a first input of a NAND gate **34***b*. The output of each of NOR gate **34***a* and NAND gate **34***b* is connected to an input of inverters **36***a* and **36***b*, respectively. Output signals A and B from inverters **36***a* and **36***b*, respectively, are applied to the gates of multiple P-channel and N-channel transistors **380***a* through **389***a* and **380***b* through **389***b*, respectively. The circuit structure of cross-coupled buffer **30** is almost the same as that of CMOS buffer **10** shown in FIG. **1A**, except that the output leads of inverters **36***a* and **36***b* are cross-coupled to other inputs of the NAND gate **34***b* and NOR gate **34***a* respectively, as shown in FIG. **3**.

When buffer **30** is receiving a logic high data input signal, P-channel transistors **380-9***a* are off and N-channel transistors **380-9***b* are on, thus effectively connecting output signal terminal **32** to ground through N-channel transistors **380-9***b* and disconnecting output signal terminal **32** from a positive supply voltage V_{DD}. Therefore a logic low output signal is provided and buffer **30** is allowed to sink a large amount of current from external circuitry (not shown) connected to terminal **32**.

Conversely, when buffer **30** is receiving a logic low data input signal, output signal terminal **32** is effectively connected to positive supply voltage V_{DD} and is disconnected from ground, therefore providing a logic high output signal and allowing buffer **10** to source a large amount of current to the external circuitry.

When the data input signal IN changes from one logic state to the other, the transient behaviors of output signals A and B respectively from inverters **36***a*, **36***b* are different from the outputs of inverters **16***a* and **16***b* of buffer **10** shown in FIG. **1A**.

When the data input signal IN changes from logic high to logic low, the output of NAND gate **34***b* changes from low to high after one NAND gate delay. Then output signal B of inverter **36***b* changes from high to low after one inverter delay, and thereafter turns off each of N-channel transistors **380-9***b*. On the other hand, when data input signal IN changes from high to low, all inputs of NOR gate **34***a* do not change to low at once. A cross-coupled second input of NOR gate **34***a* which is provided with output signal B by inverter **36***b* slowly changes to low after one NAND gate and one inverter gate delay. After that, output signal A of inverter **36***a* changes to low after one NOR gate and one inverter gate delay, and then turns on P-channel transistors **380-9***a*. Therefore, the turn-on of P-channel transistor **380***a* is delayed after the turn-off of N-channel transistor **380***b* by one NOR gate and one inverter gate delay period, thereby inhibiting overlap current.

Conversely, when data input signal IN changes from low to high, the turn-on of N-channel transistor **380***b* is delayed after the turn-off of P-channel transistor **380***a* by one NAND gate and one inverter gate delay period, to inhibit overlap current.

However, this cross-coupled output buffer **30** also has disadvantages. The delay period resulting from the cross-coupling is too long due to plural transistor feedback gates (explained below in more detail), and cannot be accurately controlled.

In the case where multiple complementary transistor pairs **380-9***a, b* are employed, the last transistors **389***a, b* turn off much later, because parasitic impedance such as resistances **37***a, b* exist between the gate of the first transistor **380***a, b* and the gate of the last transistor **389***a,*

b. The parasitic impedance typcially results, in part, from the nature of the physical layout implementation of buffer **30** which is often required to comply with certain rules, in part, to control the conventional and well documented di/dt problem. Due to the delay of the turn-off of the last transistors **389***a, b*, electrical currents pass, for example, through P-channel transistor **389***a* and N-channel transistor **380***b* during the transient periods. Accordingly, in order to eliminate such cross-flowing overlap currents, more delay of the turn-on of the transistors is required and therefore more transistors are needed to accomplish the more delay. However these transistors are expensive and difficult to install, and their delay can not be adequately controlled.

Now, reference will be made to the inside structures of an inverter, a NAND gate and a NOR gate. An inverter, such as inverters **16***a, b* shown in FIG. **1**A, is comprised of two MOS transistors as shown in FIGS. **4**A and **4**B. FIG. **4**A shows the symbol for an inverter **40** having an input terminal **41** and an output terminal **42**. FIG. **4**B shows the MOS transistor implementation of the inverter **40**. As shown in FIG. **4**B, inverter **40**, again having input terminal **41** and output terminal **42**, is constructed by suitably connecting a P-channel MOS transistor **44** and an N-channel MOS transistor **45**, with a terminal **43** being connected to a positive supply voltage. Thus, inverter **40** requires two MOS transistors. Therefore it should be understood that the circuit of FIG. **1**B is equivalent to buffer circuit **10** shown in FIG. **1**A.

Similarly, a three-input NAND gate, such as NAND gate **34***b* of FIG. **3**, requires six MOS transistors. A two-input NAND gate requires four transistors. As shown in FIGS. **5**A and **5**B, NAND gate **50**, having inputs **51** and **52** and an output **53**, is constructed utilizing P-channel MOS transistors **54** and **55**, and N-channel MOS transistors **56** and **57**, with a terminal **58** being connected to a positive supply voltage. Furthermore, a three-input NOR gate, such as NOR gate **34***a* of FIG. **3**, requires at a minimum four MOS transistors. As shown in FIGS. **6**A and **6**B, two-input NOR gate **60**, having inputs **61** and **62** and an output **63**, is constructed utilizing P-channel MOS transistors **65** and **66**, and N-channel MOS transistors **67** and **68**.

Accordingly it should be understood that the propagation delay of NOR gate **34***a* of FIG. **3** is equal to two transistor gate delays when its output changes low to high. And it also should be understood that the propagation delay of NAND gate **34***b* of FIG. **3** is equal to two transistor gate delays when its output changes high to low.

In FIG. **3**, when data input signal IN changes high to low, the turn-on of P-channel transistor **380***a* is delayed after the turn-off of N-channel transistor **380***b* by three transistor gate delay periods, which is too long and uncontrollable. Conversely, when data input signal IN changes from low to high, the turn-on of N-channel transistor **380***b* is delayed after the turn-off of P-channel transistor **380***a* by three transistor gate delay periods, which is also too long and uncontrollable.

The output buffer circuit according to the present invention will now be described in detail with reference to preferred embodiments thereof, which are illustrated in FIGS. **7** and **8**.

For convenience of explanation, certain transistor gates are specifically described as P-channel or N-channel. However, those of skill in the art will understand that theses are merely for ease of explanation and not intended to be limiting, and that the present invention includes arrangements where the channel types are inverted and/or where other combinations of P- and N-channels and voltage polarities are used. As is well understood, the FET devices of the circuit as well as other circuit components and their interconnections as illustrated may be fabricated as an integrated circuit in a single body of semiconductor material.

As shown in FIG. **7**, an output buffer circuit **70** includes a data input terminal **71** for receiving a data input signal IN, an output signal terminal **72** for providing an output signal OUT, an input stage **73**, a pre-driver stage **75**, and an output driver stage **77**. Input stage **73** comprises a NOR gate **74***a* and a NAND gate **74***b*. One input lead of NOR gate **74***a* and one input lead of NAND gate **74***b* are connected in common to receive the data input signal IN from input terminal **71**. Other input leads of both gates **74***a, b* are used for receiving control or enable signals (not shown).

Pre-driver stage **75** comprises a first stacked pair of P-channel MOS FETs **76***a* and **76***b*, and a second stacked pair of N-channel MOS FETs **76***c* and **76***d*. P-channel transistors **76***a* and **76***b* are serially connected between a supply voltage V_{DD} and a juncture of serially connected N-channel transistors **76***c* and **76***d*. N-channel Transistors **76***c* and **76***d* are serially connected between ground and a juncture of P-channel transistors **76***a* and **76***b*. The output of NOR gate **74***a* is connected to the gates of P-channel transistor **76***a* and N-channel transistor **76***c*. The output of NAND gate **74***b* is connected to the gate of P-channel transistor **76***b* and N-channel transistor **76***d*. A first output AA of pre-driver stage **75** is derived at a node between P-channel transistors **76***a* and **76***b*. A second output BB of pre-driver stage **75** is derived at a node between N-channel transistors **76***c* and **76***d*.

It should be noted that pre-driver stage **75** has the same number of transistors as buffer circuit **10** of FIGS. **1**A and **1**B. That is, implementation of pre-driver stage **75** can be accomplished by using the same number of transistors as in the known circuit but rewiring them as shown in FIG. **7**.

Output driver stage **77** comprises a complementary pair of a P-channel MOS FET **78***a* and an N-channel MOS FET **78***b*. The MOS FETs **78***a* and **78***b* are connected in series between voltage supply V_{DD} and ground. The gate of P-channel MOS FET **78***a* receives output AA from pre-driver stage **75**. The gate of N-channel MOS FET **78***b* receives output BB from pre-driver stage **75**. The output signal OUT is derived at a juncture of MOS FETs **78***a* and **78***b*.

In operation, when data input signal IN at input terminal **71** changes from logic low to high, the logic high signal is applied to a first input of NOR gate **74***a* thereby causing NOR gate **74***a* to generate a logic low signal at its output which is connected to the gates of transistors **76***a* and **76***c*. An enable signal M is at a logic low. Thus, P-channel transistor **76***a* turns on (conductive) and N-channel transistor **76***c* turns off (nonconductive), thus changing output AA to high immediately. High output AA is applied to the gate of P-channel transistor **78***a*, thus causing P-channel transistor **78***a* to turn off.

Simultaneously, the logic high input signal IN is applied also to a first input of NAND gate **74***b* with the other input lead receiving a logic high enable signal N, thereby causing NAND gate **74***b* to provide a logic low signal at its output which is connected to the gates of transistors **76***b* and **76***d*. Thus, P-channel transistor **76***b*

turns on and N-channel transistor **76***d* turns off. Output BB becomes high at a delay period after output AA becomes high. This is because two stacked transistors **76***a* and **76***b* must turn on thereby providing output BB as a logic high while transistor **76***a* must turn on for output AA to be a logic high.

Therefore, N-channel transistor **78***b* does not become conductive until P-channel transistor **78***a* is completely nonconductive, thereby inhibiting overlap current. This delay period is determined by the sizes, especially the width-to length ratios (W/L), of transistors **76***a*, **76***b*; therefore it can be controlled.

Conversely, when data input signal IN at input terminal **71** changes from a logic high to low, the logic low signal is applied to the first input of NAND gate **74***b* thereby causing NAND gate **74***b* to generate a logic high signal at its output which is connected to the gates of transistors **76***b* and **76***d*. Thus, N-channel transistor **76***d* turns on and P-channel transistor **76***b* turns off, thereby changing output BB immediately to a logic low. Logic low output BB is applied to the gate of N-channel transistor **78***b*, thus causing N-channel transistor **78***b* to turn off.

Simultaneously, the logically low input signal IN is applied also to the first input of NOR gate **74***a* with the second input receiving a low enable signal M, thereby causing NOR gate **74***a* to generate a logic high signal on its output which is connected to the gates of transistors **76***a* and **76***c*. Thus, P-channel transistor **76***a* turns off and N-channel transistor **76***c* turns on. Output AA becomes low at a delay period after output BB becomes low. This is because two stacked or series-connected transistors **76***c* and **76***d* must turn on to provide a low output AA while only one transistor **76***d* must turn on for a low output BB.

Therefore, P-channel transistor **78***a* does not become conductive until N-channel transistor **78***b* is completely shut off, thereby inhibiting the overlap current. This delay period is determined by the transistor sizes, especially the width-to length ratios (W/L), **76***c*, **76***d*; therefore the delay can be controlled. That is, the transient period of transistor **78***a* does not overlap with the transient period of transistor **78***b*. Thus output buffer circuit **70** provides no or significantly reduced overlap current and less noise by turning off the active output transistor before turning on the opposing output transistor. By controlling the width-to length ratios (W/L) of transistors in pre-driver stage **75**, the delay period can be very easily controlled. This pre-driver structure can be easily retrofit into existing output buffer designs.

FIG. **8** shows another embodiment according to the present invention. An output buffer circuit **80** includes a data input terminal **81** for receiving an input data signal IN, an output signal terminal **82** for providing an output signal OUT, an input stage **83**, a pre-driver stage **85**, and an output driver stage **87**. The circuit structure of output buffer **80** of this embodiment is almost the same as that of the first embodiment buffer **70** shown in FIG. **7** except that output driver stage **87** includes a predetermined number of plural pairs of P-channel and N-channel MOS transistors **880***a, b* through **889***a, b*, as noted by the dashed lines. Output buffer **80** further comprises assist transistors **89**.

In the illustrated form, assist transistors **89** include P-channel MOS FETs **890***a* through **899***a*, and N-channel MOS FETs **890***b* through **899***b*. P-channel transistor **899***a*, for example, is placed near the gate of corresponding P-channel transistor **889***a* to enhance the turn-off of transistor **889***a*. Other assist transistors **890** through **899** are placed near the gates of corresponding transistors **880** through **889**. The gate of P-channel transistor **899***a* is connected to an output of NOR gate **84***a*, its source is connected to a positive supply voltage V_{DD}, and its drain is connected to the gate of transistor **889***a*.

It should be apparent from the previous discussion that significant impedance such as parasitic resistance **87***a* exists between the gate of transistor **880***a* and transistor **889***a*. This impedance causes overlap currents by slowing down the turn-off of the opposite drivers, as described above with reference to FIG. **3**. Assist transistor **899***a* compensates the slowing down of the turn-off of opposite transistor **889***a* caused by the impedance, and facilitates the quick turn-off of transistor **889***a*. Other assist transistors may be similarly connected and function similarly. Assist transistors **890***a, b* through **899***a, b* are responsible for the turn-off direction only.

In this way, the combination of the stacked pre-driver transistors and the assist devices provide a faster and quieter output buffer circuit relative to what is conventionally used in CMOS applications. The output buffer circuit according to the invention provides great reduction in overlap current, RFI noise and power consumption.

While the present invention has been shown and described with reference to particular embodiments thereof, various modifications and changes thereto will be apparent to those skilled in the art and are within the spirit and scope of the present invention.

I claim:

1. An output buffer circuit having a data input terminal for receiving a data signal, and an output signal terminal for providing an output signal, comprising:

an input stage for receiving the data signal from the data input terminal and for providing input stage outputs;

a pre-driver stage for receiving the input stage outputs and for providing first and second outputs in response to the input stage outputs, said first output becoming logically low after a first predetermined controlled delay period after said second output becomes logically low, and said second output becoming logically high after a second predetermined controlled delay period after said first output becomes logically high; and

an output driver stage for receiving said first and second outputs from the pre-driver stage and for providing the output signal to the output signal terminal, said output driver stage including at least one complementary pair of serially connected output transistor devices, and said output signal being derived at a node between said serially connected output transistor devices,

said first and second outputs of the pre-driver stage being supplied only to said output driver stage and not to said input stage.

2. An output buffer circuit according to claim **1** wherein said input stage comprises a first logic gate and a second logic gate each having at least one input and an output, said inputs of the first and second logic gates being connected together for receiving the data signal.

3. An output buffer circuit according to claim **1** wherein said pre-driver stage comprises:

a first pair of transistors being serially connected between a first supply voltage terminal and said second output of the pre-driver stage, a node be-

tween said first pair of transistors being connected to said first output of the pre-driver stage; and

a second pair of transistors being serially connected between said first output of the pre-driver stage and a second supply voltage terminal, a node between said second pair of transistors being connected to said second output of the pre-driver stage.

4. An output buffer circuit according to claim **3** wherein control electrodes of said first and second pairs of transistors are connected to the input stage outputs.

5. An output buffer circuit according to claim **4** wherein said first pair of transistors are MOS transistors of a first conductivity, and said second pair of transistors are MOS transistors of a second conductivity.

6. An output buffer circuit according to claim **5** wherein said first conductivity is a p-type conductivity, and said second conductivity is an n-conductivity.

7. An output buffer circuit according to claim **3** wherein:

said first predetermined controlled delay period is determined by width-to-length ratios (W/L) of said second pair of transistors; and

said second predetermined controlled delay period is determined by width-to-length ratios (W/L) of said first pair of transistors.

8. An output buffer circuit according to claim **1** wherein:

said at least one complementary pair of output transistor devices comprises a p-channel MOS transistor and an n-channel MOS transistor.

9. An output buffer circuit according to claim **8** wherein:

a source of said p-channel MOS transistor is connected to a first supply voltage terminal;

a gate of said p-channel MOS transistor receives said first output from the pre-driver stage;

drain electrodes of both of said p-channel and n-channel MOS transistors are connected together for providing the output signal;

a gate of said n-channel MOS transistor receives the second output from the pre-driver stage; and

a source of said n-channel transistor is connected to a second supply voltage terminal.

10. An output buffer circuit having a data input terminal for receiving a data signal, and an output signal terminal for providing an output signal, comprising:

an input stage for receiving the data signal from the data input terminal and for providing input stage outputs;

a pre-driver stage for receiving the input stage outputs and for providing first and second outputs in response to the input stage outputs, said first output becoming logically low at a first predetermined controlled delay period after said second output becomes logically low, and said second output becoming logically high at a second predetermined controlled delay period after said first output becomes logically high;

an output driver stage including a plurality of complementary pairs of serially connected p- and n-channel MOS transistors, said plurality of pairs being connected in parallel between first and second supply voltage terminals, control electrodes of said p-channel transistors receiving said first output from the pre-driver stage, control electrodes of said n-channel transistors receiving said second output from the pre-driver stage, and all nodes between said MOS transistors in said pairs being connected together for providing the output signal to the output signal terminal; and

assist means for receiving the input stage outputs and for assisting said MOS transistors in turning off,

said first and second outputs of the pre-driver stage being supplied only to said output driver stage and not to said input stage.

11. An output buffer circuit according to claim **10** wherein:

said input stage comprises a first logic gate and a second logic gate each having at least one input and an output, said inputs of the first and second logic gates being connected in common for receiving the data signal.

12. An output buffer circuit according to claim **10** wherein said pre-driver stage comprises:

a first pair of transistors being serially connected between a first voltage supply and said second output of the pre-driver stage, a node between said first pair of transistors being connected to said first output of the pre-driver stage; and

a second pair of transistors being serially connected between said first output of the pre-driver stage and a second voltage supply, a node between said second pair of transistors being connected to said second output of the pre-driver stage.

13. An output buffer circuit according to claim **12** wherein:

said assist means further comprise MOS transistors having gates connected to the input stage outputs, said assist means supplying signals for turning off the MOS transistors in the output driver stage.

14. An output buffer circuit according to claim **12** wherein:

said first predetermined controlled delay period is determined by width-to-length ratios (W/L) of said second pair of transistors; and

said second predetermined controlled delay period is determined by width-to-length ratios (W/L) of said first pair of transistors.

* * * * *

EXHIBIT B

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United States Patent [19]

Tam et al.

[11] Patent Number: 5,105,250

[45] Date of Patent: Apr. 14, 1992

[54] **HETEROJUNCTION BIPOLAR TRANSISTOR WITH A THIN SILICON EMITTER**

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[73] Assignee: **Motorola, Inc.**, Schaumburg, Ill.

[21] Appl. No.: **594,576**

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[51] **Int. Cl.**[5] **H01L 29/72**; H01L 29/161; H01L 29/04

[52] **U.S. Cl.** **357/34**; 357/35; 357/16; 357/59

[58] **Field of Search** ..... 357/35, 34, 16, 59 H

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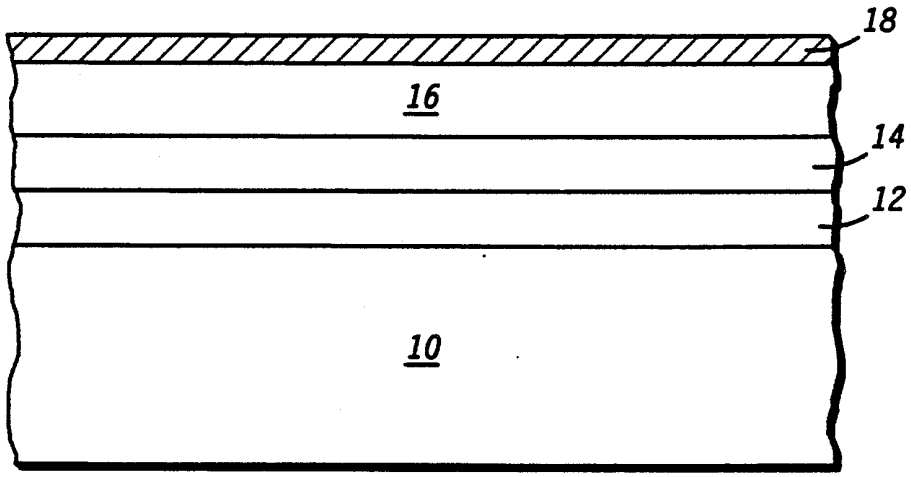
Assistant Examiner—Wael Fahmy
Attorney, Agent, or Firm—Miriam Jackson; Joe E. Barbee

[57] **ABSTRACT**

A heterojunction bipolar transistor having a thin, lightly doped, silicon emitter disposed on a silicon-germanium base layer exhibits low emitter resistance and low emitter-base capacitance. The lightly doped silicon emitter maintains the bandgap differential between silicon-germanium and silicon. The silicon emitter is fabricated such that the silicon emitter will be substantially depleted at zero bias, resulting in low emitter-base resistance and emitter resistance.

10 Claims, 1 Drawing Sheet



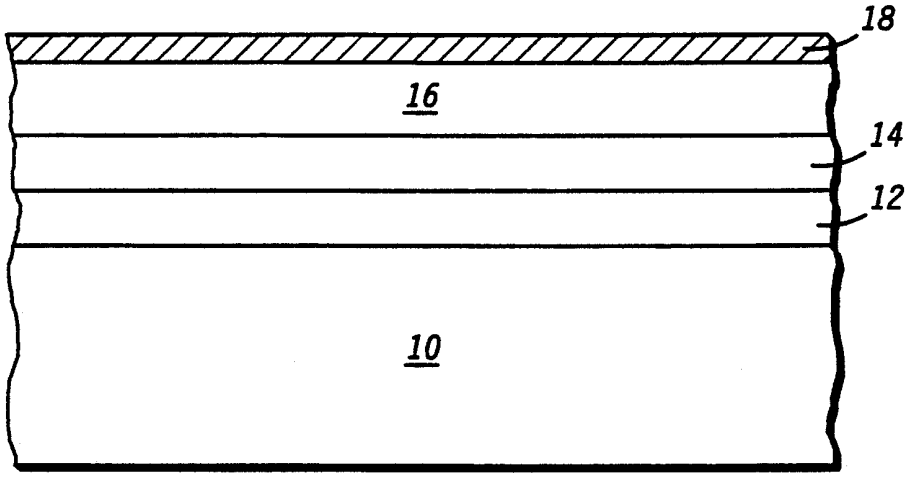
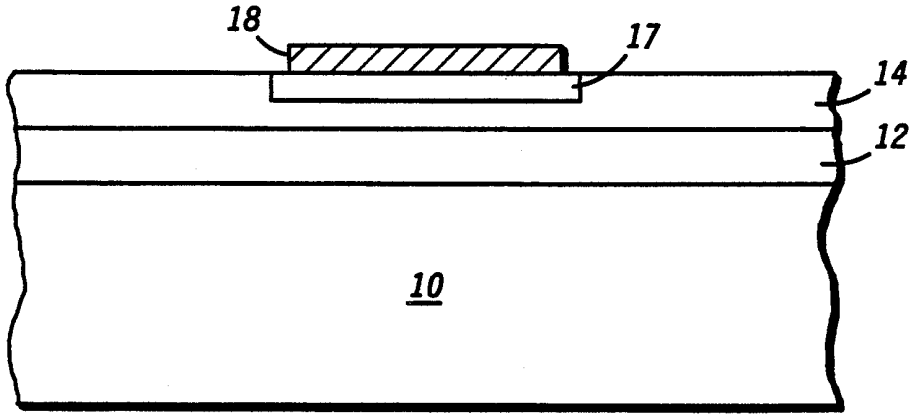


FIG. 1

FIG. 2



HETEROJUNCTION BIPOLAR TRANSISTOR WITH A THIN SILICON EMITTER

BACKGROUND OF THE INVENTION

This invention relates, in general, to semiconductor devices, and more particularly, to a heterojunction bipolar transistor.

Heterojunction bipolar transistors exhibit electrical characteristics which are advantageous over the electrical characteristics of homojunction bipolar transistors. Silicon-germanium heterojunction bipolar transistor processing is compatible with existing silicon processing. Thus, silicon-germanium heterojunction bipolar transistors are preferred over other heterojunction bipolar transistors. In particular, silicon-germanium heterojunction bipolar transistors exhibit high emitter injection efficiency, reduced charge storage in the emitter, reduced or eliminated hole injection into the emitter. These characteristics are obtained because of the bandgap differential between the silicon and silicon-germanium metallurgical junction.

A silicon-germanium heterojunction bipolar transistor of the prior art consists of an N-type silicon collector, a P-type silicon-germanium base, and an N-type polysilicon layer. The N-type dopant from the polysilicon is diffused into the base to form an emitter region. The problem with this structure is that boron diffuses into the polysilicon layer or arsenic diffuses into the silicon-germanium base during the formation of the emitter. This diffusion degrades the bandgap differential by moving the metallurgical junction from the silicon-germanium and polysilicon interface into either the polysilicon layer or into the silicon-germanium base. Thus, the advantageous electrical characteristics described above are not exhibited.

A way of maintaining the metallurgical junction at the silicon-germanium and polysilicon interface is to prevent the diffusion of boron or arsenic from the respective layers. A structure in which the polysilicon layer is used as the emitter would solve this problem because the diffusion of boron or arsenic can be prevented. However, in this structure, the interface between the polysilicon layer and the silicon-germanium layer is poor, which results in the transistor exhibiting poor electrical characteristics, such as high leakage.

A transistor which solves this interface problem has been disclosed by King et al, in an article entitled, "Si/$Si_{1-x}Ge_x$ Heterojunction Bipolar Transistors Produced by Limited Reaction Processing," published in IEEE Electron Device Letters, Vol. 10, No. 2, on Feb. 1989. The use of a thick silicon emitter of approximately 4,000 angstroms in thickness, instead of the polysilicon emitter eliminates the interface problem, and maintains the bandgap differential between the silicon-germanium layer and the silicon emitter layer in this case. However, in this structure, the thick silicon emitter must be lightly doped to avoid breakdown voltage problems and to avoid high emitter-base capacitance. A lightly doped, thick emitter exhibits high emitter resistance. Thus, it would be desirable to fabricate a heterojunction bipolar transistor in which the bandgap differential is ensured and also where emitter resistance and capacitance is low.

Accordingly, it is an object of the present invention is to provide an improved heterojunction bipolar transistor.

Another object of the present invention is to provide a heterojunction bipolar transistor having low emitter-base capacitance and low emitter resistance.

A further object of the present invention to provide a heterojunction bipolar transistor in which the bandgap differential between silicon and silicon-germanium is maintained.

SUMMARY OF THE INVENTION

The above and other objects and advantages of the present invention are achieved by a heterojunction bipolar transistor having a thin, lightly doped, silicon emitter disposed on a silicon-germanium base layer. The lightly doped silicon emitter maintains the bandgap differential between silicon-germanium and silicon. The silicon emitter is fabricated such that it will be depleted at zero bias so that emitter-base capacitance and emitter resistance is low. In one embodiment, a polysilicon contact layer may be formed on the silicon emitter and can be heavily doped to further reduce emitter resistance. In a second embodiment, a thin ohmic contact region may be formed in the silicon emitter instead of the polysilicon contact layer.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 illustrates an enlarged, cross-sectional portion of a first embodiment of the present invention; and

FIG. 2 illustrates an enlarged, cross-sectional portion of a second embodiment of the present invention.

DETAILED DESCRIPTION OF THE INVENTION

FIG. 1 illustrates an enlarged, cross-sectional view of a portion of a heterojunction bipolar transistor in a first embodiment of the present invention. What is shown is a silicon layer **10** which acts as the collector of the heterojunction bipolar transistor, a silicon-germanium layer **12** which acts as the base, a thin silicon layer **14** formed on the silicon-germanium layer **12** which acts as the emitter, and a polysilicon layer **16** which acts as the emitter contact. A metal contact layer **18** is formed on polysilicon layer **16**.

Silicon collector layer **10** is preferably doped N-type, using arsenic or antimony as a dopant. Silicon-germanium base layer **12** is preferably doped P-type, using boron as a dopant at approximately 1×10^{19} to 3×10^{19} atoms/cm^3. The thickness of silicon-germanium base layer **12** is preferably approximately 500 angstroms. Thin silicon layer **14** is preferably lightly doped N-type, using arsenic as a dopant at approximately 8×10^{16} to 3×10^{17} atoms/cm^3. The thickness of silicon layer **14** is preferably approximately 500 to 1500 angstroms. The thickness and doping of silicon layer **14** should be chosen such that silicon layer **14** will be substantially depleted at zero bias during normal operation. This is necessary in order to reduce emitter-base capacitance and emitter resistance. If silicon layer **14** is too thick, for example 4,000 angstroms as is described in the prior art, silicon layer **14** will not be depleted at zero bias and emitter resistance will be high. Polysilicon layer **16** is preferably heavily doped N-type using arsenic as a dopant.

After doping polysilicon layer **16**, it is critical to anneal the heterojunction bipolar transistor by rapid thermal anneal to prevent degradation of the bandgap differential of silicon layer **14** and silicon-germanium layer **12** by preventing the diffusion of arsenic and boron from silicon-germanium layer **12** and silicon layer

14. Polysilicon layer 16 is heavily doped in order to further lower emitter resistance. In a preferred embodiment, polysilicon layer 16 is doped using arsenic as a dopant at a level of approximately greater than 1×10^{19} atoms/cm^3. The above layers are formed using techniques well known in the art. Note that only the active region of a heterojunction bipolar transistor is shown and described, however, this structure may be readily incorporated into many heterojunction bipolar process.

By including silicon layer 14 the metallurgical junction will be at the interface between silicon layer 14 and silicon-germanium layer 12. Thus, the advantage of the bandgap differential is not lost as in the prior art. In addition, the heterojunction bipolar transistor of the present invention has low emitter resistance and low emitter-base capacitance. The low emitter resistance is obtained by forming a heavily doped polysilicon layer 16. The low emitter-base capacitance is obtained by designing silicon layer 14 to be substantially depleted during operation. The heterojunction bipolar transistor of the present invention is thus a very high speed device that can be used for high speed digital and microwave applications.

FIG. 2 illustrates an enlarged, cross-sectional view of a portion of a heterojunction bipolar transistor in a second embodiment of the present invention. The same elements shown in FIG. 1 are referenced by the same numerals. FIG. 2 illustrates a structure similar to that of FIG. 1, however, in FIG. 2 polysilicon layer 16 is not utilized. In addition, silicon layer 14 is preferably slightly thicker than in FIG. 1. Silicon layer 14 is preferably approximately 1,000 to 2,500 angstroms so that a shallow emitter contact region 17 may be formed therein. Emitter contact region 17 is preferably formed by using a heavy dose of arsenic, and is just deep enough to provide ohmic contact to metal layer 18. In this second embodiment, as in the first embodiment, silicon emitter layer 14 is thin enough so that it is substantially depleted during operation. Thus, the structure of FIG. 2 also exhibits good electrical properties.

As can be readily seen, the heterojunction bipolar transistor of the present invention maintains the bandgap differential, thus exhibits high emitter injection efficiency, reduced charge storage in the emitter, reduced or eliminated hole injection into the emitter. In addition the heterojunction bipolar transistor of the present invention exhibits low emitter resistance and emitter-base capacitance by utilizing a thin silicon emitter layer.

We claim:

1. A heterojunction bipolar transistor, comprising:
a collector;
a silicon-germanium base disposed on the collector;
a thin silicon emitter disposed on the silicon-germanium base, wherein a metallurgical junction is maintained at the silicon-germanium base and the thin silicon emitter interface; and
a polysilicon layer disposed on the thin silicon emitter.

2. The heterojunction bipolar transistor of claim 1 wherein the silicon emitter is of a thickness where the thin silicon emitter is substantially depleted at zero bias.

3. The heterojunction bipolar transistor of claim 2 wherein the silicon emitter is of a thickness of approximately 500 to 2,500 angstroms.

4. A heterojunction bipolar transistor comprising:
a collector;
a silicon-germanium base formed on the collector;
a thin silicon emitter formed on the silicon-germanium base, wherein the silicon emitter has a thickness and a doping level such that it is substantially depleted during normal operation, and wherein a metallurgical junction is maintained at the silicon-germanium base and the thin silicon emitter interface; and
a polysilicon layer formed on the silicon layer.

5. The heterojunction bipolar transistor of claim 4 wherein the silicon emitter is of a thickness of approximately 500 to 2,500 angstroms.

6. The heterojunction bipolar transistor of claim 4 wherein the polysilicon layer is heavily doped.

7. A heterojunction bipolar transistor, comprising:
an N-type collector;
a P-type silicon-germanium base formed on the collector;
an N-type, thin, lightly doped silicon emitter formed on the silicon-germanium base, wherein a metallurgical junction is maintained at the P-type silicon-germanium base and the N-type, thin, lightly doped silicon emitter interface; and
an N-type, heavily doped polysilicon layer formed on the silicon layer.

8. The heterojunction bipolar transistor of claim 7 wherein the thin, lightly doped silicon emitter is substantially depleted during normal operation.

9. The heterojunction bipolar transistor of claim 8 wherein the thin, lightly doped silicon emitter is doped at approximately 8×10^{16} to 3×10^{17} atoms/cm^3.

10. The heterojunction bipolar transistor of claim 7 wherein the heavily doped polysilicon layer is doped at approximately 1×10^{19} atoms/cm^3.

* * * * *

EXHIBIT C

US005172214A

United States Patent [19]

Casto

[11] Patent Number: 5,172,214

[45] Date of Patent: Dec. 15, 1992

[54] **LEADLESS SEMICONDUCTOR DEVICE AND METHOD FOR MAKING THE SAME**

[75] Inventor: **James J. Casto**, Austin, Tex.

[73] Assignee: **Motorola, Inc.**, Schaumburg, Ill.

[21] Appl. No.: **866,282**

[22] Filed: **Apr. 10, 1992**

Related U.S. Application Data

[63] Continuation of Ser. No. 651,165, Feb. 6, 1991, abandoned.

[51] **Int. Cl.**[5] **H01L 23/28**; H01L 21/56

[52] **U.S. Cl.** **257/676**; 437/211; 437/220; 437/902; 257/693; 257/796; 257/737

[58] **Field of Search** 357/72, 68, 69, 70, 357/81; 437/211, 220, 902

[56] **References Cited**

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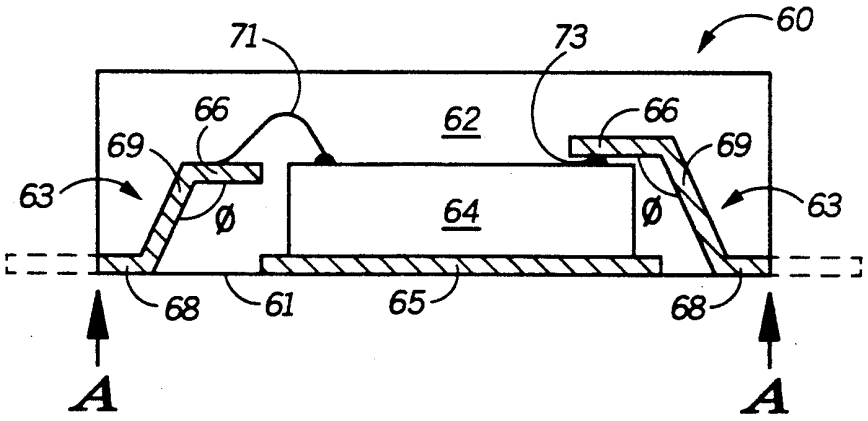
Primary Examiner—Edward J. Wojciechowicz
Attorney, Agent, or Firm—Patricia S. Goddard

[57] **ABSTRACT**

A semiconductor device having a thin package profile is leadless, thereby minimizing necessary mounting space on a substrate. In one form, a semiconductor device has a semiconductor die electrically coupled to a plurality of conductive leads. Each lead has a first portion, a second portion, and an intermediate portion which separates the first and second portions. A package body encapsulates the semiconductor die and the first and intermediate portions of the leads. The second portions of the leads are exposed on the bottom surface of the package body and are used to electrically access the semiconductor die.

12 Claims, 1 Drawing Sheet



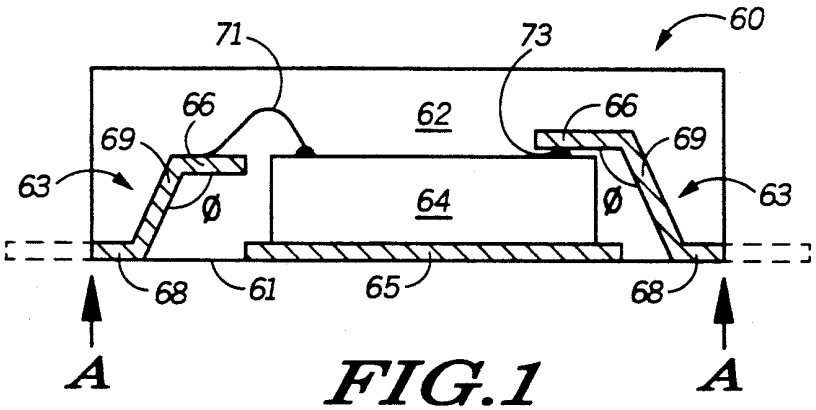


FIG.1

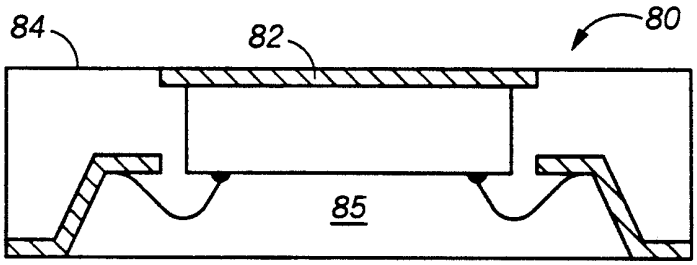


FIG.2

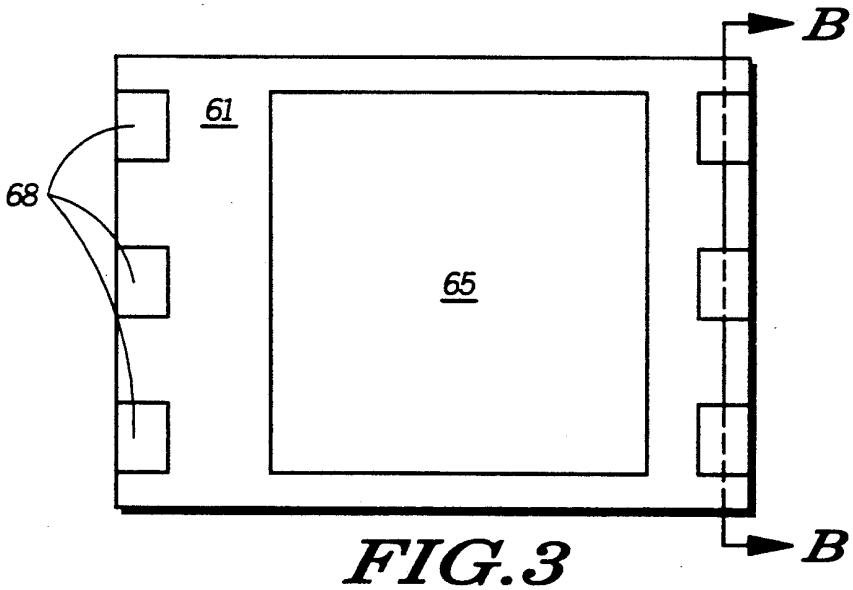


FIG.3

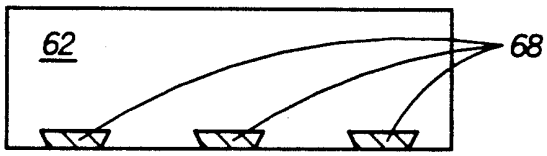


FIG.4

LEADLESS SEMICONDUCTOR DEVICE AND METHOD FOR MAKING THE SAME

This application is a continuation of prior application Ser. No. 07/651,165, filed Feb. 6, 1991, now abandoned.

CROSS-REFERENCE TO RELATED APPLICATION

This application is related to a commonly assigned co-pending patent application entitled, "SEMICONDUCTOR DEVICE HAVING DUAL ELECTRICAL CONTACT SITES AND METHOD FOR MAKING THE SAME," by McShane et al., Ser. No. 07/651,166, filed concurrently herewith.

TECHNICAL FIELD OF THE INVENTION

The present invention is related to semiconductor devices in general, and more specifically, to leadless semiconductor devices having thin package profiles and a method for making the same.

BACKGROUND OF THE INVENTION

In order to meet the demands of the growing electronics industry, semiconductor manufacturers are faced with many challenges in supplying suitable semiconductor devices. One challenge is to provide customers with very small, yet powerful, devices. However, this challenge is not easily met. Small devices are desirable because small devices require less mounting space on a substrate and have fewer problems with signal transmissions as compared to larger devices. At the same time, powerful devices are necessary in order to store and transmit a maximum amount of imformation. Yet as the power and performance of a device increases, the size of the device also increases. Much of this increase is due to a larger number of terminals, or leads, required to operate the device.

Keeping the size of a semiconductor device to a minimum is often achieved by using thin, fragile, densely spaced leads as electrical contacts to the device. However, the use of such leads creates a variety of manufacturing and handling problems. Handling devices with such fragile leads can result in bent and non-coplanar leads, making it difficult to properly mount the device to a substrate, such as a PC (printed circuit) board. Manufacturing devices with such closely spaced leads is itself difficult. Leadframes used in molded packages have a piece of metal, known as a dambar, to act as a dam for molding material. The dambar must be cut out from between the leads prior to using the device, usually by a punching operation. Closely spaced leads can be damaged by the punching operation. Furthermore, the small dimensions of a punching tool used for removing dambars from between fine leads make the punching tool susceptible to damage as well.

Although much of the effort devoted to reducing package size has concentrated on reducing the package width and length, it is also desirable for semiconductor devices to be thin, especially in consumer electronics applications. Therefore, a need exists for an improved semiconductor device, and more specifically for an improved semiconductor device which is leadless and has a thin package profile.

BRIEF SUMMARY OF THE INVENTION

The previously mentioned needs are fulfilled, and other advantages are achieved with the present invention. In one form, a semiconductor device has a semiconductor device die. The semiconductor device die is electrically coupled to a plurality of conductive leads. Each lead has a first portion and a second portion, the first portion being separated from the second portion by an intermediate portion. A package body encapsulates the semiconductor device die and first and intermediate portions of the plurality of conductive leads. The second portions of the plurality of conductive leads are exposed on an edge and a bottom surface of the package body.

BRIEF DESCRIPTION OF THE FIGURES

FIG. **1** illustrates, in cross-section, an embodiment of a semiconductor device in accordance with the present invention.

FIG. **2** illustrates, in cross-section, another embodiment of a semiconductor device in accordance with the present invention.

FIG. **3** illustrates, in planar view, the bottom surface of the semiconductor device of FIG. **1**.

FIG. **4** illustrates, in cross-section, a view of the semiconductor device of FIG. **3** taken along the line B—B.

DETAILED DESCRIPTION OF A PREFERRED EMBODIMENT

The present invention has several advantages over conventional semiconductor devices. One advantage is that a semiconductor device in accordance with the present invention is externally leadless. Most known devices have leads which are external to a package body. The presence of external leads requires that a device occupy more space on a substrate, such as a printed circuit board, than if the device had no external leads. Furthermore, the presence of leads generates handling and manufacturing problems as discussed earlier. Some known semiconductor devices are considered to be leadless, for example a leadless chip carrier (LCC). However, most LCCs are formed from a multilayer ceramic material, and therefore LCCs are quite expensive. An overmolded device is also leadless, but overmolded devices require a semiconductor die to be mounted onto a PC board prior to encapsulation. Since an overmolded device contains a portion of a PC board, the cost of the device is significantly increased.

Another advantage of the present invention is that a semiconductor device can be made very thin, up to half the thickness of many conventional devices. Thin semiconductor devices are a competitive advantage in the consumer market for such applications as smart cards, cellular telephones, and pagers. Yet another advantage is that the present invention also allows a semiconductor device to have good heat dissipation, without increasing the size of the device. Heat dissipation is an important concern in high performance and high power consumption devices. Most methods of removing heat from a device, such as using heat sinks, increase the size of the device. The present invention can effectively dissipate heat without an increase in device size.

Illustrated in FIG. **1** is a semiconductor device **60** in accordance with the present invention. Device **60** has a semiconductor device die **64** which is usually an integrated circuit. Also included in device **60** is a leadframe (not entirely shown) having a plurality of leads **63** and a die receiving area **65** also known as a die pad or flag. Conventional leadframe materials, such as copper, copper alloys, iron-nickel alloys, or TAB (tape automated bonding) leadframes, are suitable for use with the pres-

ent invention. Semiconductor device die **64** is positioned at die receiving area **65**, typically using an adhesive material, and is electrically coupled to the plurality of leads **63**. The left portion of device **60** illustrated in FIG. **1** uses a wire bond **71** to couple a lead to the die, whereas the right portion of device **60** illustrates use of a TAB bond **73** or other type of lead-on-chip bond. Usually a semiconductor device contains only one type of coupling technique. The device of FIG. **1** has two different coupling techniques solely for illustrative purposes.

Device **60** is approximately one-half the thickness of a conventional molded semiconductor device. Most semiconductor devices have a package body which extends both above and below a plurality of leads of a leadframe. The device illustrated in FIG. **1** is thinner than many known devices because a protective package body **62** is formed only above the plurality of leads **63** of the leadframe. This is accomplished by forming the package in a one-sided mold tool or a mold tool having one planar platen. Typically, molded semiconductor device packages are formed in mold tools having an upper and a lower platen, each platen having a cavity. The platens are brought together such that the two cavities form a larger cavity which surrounds a semiconductor device die and inner portions of leads of a leadframe. An encapsulating material is introduced into the larger cavity to form a package body which completely surrounds a die and inner portions of the leads. The package body extends both above and below the die and the leads. Device **60**, on the other hand, has package body **62** only formed above the leads **63** and semiconductor device die **64**.

In accordance with the present invention, the leads **63** of device **60** in FIG. **1** have first portions **66**, second portions **68**, and intermediate portions **69**. Second portions **68** of leads **63** are exposed on a bottom surface **61** of package body **62** and on the sides of the package body. Upon forming package body **62** about semiconductor device die **64**, leads **63** will extend from the package body, as illustrated by the dashed lines in FIG. **1**. The leads may then be formed into standard lead configurations, such as gull-wing, J-lead, through-hole, or the like. Preferably, leads **63** are severed at points A to create a leadless semiconductor device. Electrical contact to the semiconductor device is made through the second portions exposed on bottom surface **61** of the package.

As illustrated in FIG. **1**, first portions **66** of leads **63** are portions of the leads which are electrically coupled to semiconductor device die **64**. In the case of wire bond coupling, it is advantageous to have the bonding surface of a lead in the same plane as the bonding surface of the die. Naturally for the TAB bond illustrated, one surface must lie just above the other. Lead-on chip bonding may also be used in accordance with the present invention. Intermediate portions **69** of the leads are portions of the leads which join first portions **66** and second portions **68**. In order to have the second portions of the leads exposed on the bottom surface of the package, yet have first portions coupled to the die, intermediate portions are at an angle with respect to both the first and second portions. For example, intermediate portions **69** of FIG. **1** are at an angle ϕ from first portions **66**. Suitable angles for use with the present invention are substantially in the range of 90°–150°, although other obtuse angles could be used.

FIG. **1** also illustrates that die receiving area **65** is exposed on the bottom surface **61** of package body **62**. Having the die receiving area, also referred to as a flag, exposed on a surface of the package improves the thermal performance of the device. Heat is conducted from semiconductor device die **64** through die receiving area **65** to the ambient, thereby reducing the temperature of the device.

To further enhance thermal performance, a die receiving area could be exposed on the top surface of the package body. Because the bottom surface of the package is adjacent to a substrate, such as a PC board, heat dissipation can be improved by removing heat through the top surface of the package rather than through the bottom surface. A semiconductor device **80**, illustrated in FIG. **2**, in accordance with the present invention, has a die receiving area **82** exposed on a top surface **84** of a package body **85**. Device **80** has a thin package profile similar to the device illustrated in FIG. **1**, yet has the added benefit of allowing heat to dissipate from a top surface which will be more exposed to the ambient.

A semiconductor device in accordance with the present invention, such as device **60** of FIG. **1**, can be mounted to a substrate, such as a printed circuit board, like other leadless devices. For example, a PC board is screen printed with a solder paste in a pattern which corresponds to the pattern of the exposed second portions of the leads. The device is then appropriately positioned on the PC board and the solder is reflowed. For more reliable board mounting, the exposed portions of the leads of the device can be pretinned or solder plated prior to mounting the device. This improves the wettability of the exposed portions of the leads and provides better coupling to the screen printed solder on the substrate. An alternative method of mounting a device in accordance with the present invention is with the use of solder balls. Solder balls could be attached to the exposed portions of the leads and then coupled to a substrate at a later point.

Illustrated in FIG. **3** is a bottom perspective of the semiconductor device illustrated in FIG. **1**. Die receiving area **65** is exposed on bottom surface **61** of the package body. Also exposed on bottom surface **61** are second portions **68** of the leads. Second portions **68** are used to electrically access the semiconductor die (not shown) and are usually electrically coupled to a substrate, for example, by solder, solder balls, gold bumps, or the like. A cross-section of second portions **68** taken along the line B—B of FIG. **3** is illustrated in FIG. **4**. The cross-sectional shape of second portions **68** is illustrated as being trapezoidal. While a trapezoidal shape is not an essential aspect of the present invention, it may be helpful to have a lead shape which secures or locks the leads into place in package body **62**. Because more of the lead is exposed on the surface of the package than in conventional semiconductor devices, added features to keep leads in place may be necessary.

Thus it is apparent that there has been provided, in accordance with the invention, a leadless semiconductor device and a method for making the same that fully meets the advantages set forth previously. Although the invention has been described and illustrated with reference to specific embodiments thereof, it is not intended that the invention be limited to these illustrative embodiments. Those skilled in the art will recognize that modifications and variations can be made without departing from the spirit of the invention. For example, use of the invention is not limited to use in packages

having one semiconductor die, but may also be used with multiple component semiconductor devices. Nor is it necessary that a device in accordance with the invention have an exposed die receiving area. Furthermore, the invention is not limited to using the electrical coupling methods described or illustrated. Likewise, any method of mounting a semiconductor device having a structure in accordance with the invention is suitable. It is not intended that the invention be limited to the substrate mounting techniques described. Therefore, it is intended that this invention encompass all such variations and modifications as fall within the scope of the appended claims.

I claim:

1. A leadless semiconductor device comprising:

a leadframe having a die receiving area and a plurality of leads extending outwardly from positions adjacent the die receiving area, each of the leads having first and second portions and an intermediate portion, the first portion of each lead being closer to the die receiving area than the second portion, and each of the first and second portions being separated by the intermediate portion thereof;

a semiconductor die positioned at the die receiving area of the leadframe and electrically coupled to the plurality of leads; and

a package body having a top surface, a bottom surface, and a perimeter, wherein the semiconductor die, the plurality of leads, and the die receiving area are completely contained within the package body and wherein a first surface of each of the second portions of the leads and an entire surface of the die receiving area are exposed on and substantially flush with one of either the top surface or bottom surface of the package body.

2. The semiconductor device of claim **1** wherein a second surface of each of the second portions of the leads is exposed on and substantially flush with the perimeter of the package body and wherein only the first and second surfaces of the leads are exposed.

3. The semiconductor device of claim **1** further comprising means for electrically coupling the second portions of the leads exposed on the bottom surface of the package body to a substrate.

4. The semiconductor device of claim **3** wherein the means for electrically coupling the second portions of the leads to a substrate comprises solder.

5. A leadless semiconductor device comprising:

a semiconductor die;

a plurality of conductive leads electrically coupled to the semiconductor die, each lead having a first portion for electrical connection to the die and a second portion for subsequent electrical connection to the device, the second portion being separated from the first portion by an intermediate portion; and

a molded package body completely containing the semiconductor die and the plurality of conductive leads wherein a first surface of each second portion is exposed on, and substantially flush with, a side of the package body and a second surface of each second portion is exposed on, and substantially flush with one of either a top surface or a bottom surface of the package body and wherein only the first and second surfaces of the leads are exposed.

6. The semiconductor device of claim **5** further comprising a die receiving area for receiving the semiconductor die and wherein a surface of the die receiving area is exposed on and flush with one of either a top surface of the package body or the bottom surface of the package body.

7. The semiconductor device of claim **5** wherein the first portions of the leads and the second portions of the leads are positioned in substantially parallel planes.

8. The semiconductor device of claim **5** wherein the first portion of each of the plurality of leads intersects the intermediate portion at an obtuse angle.

9. A method for fabricating a leadless semiconductor device comprising the steps of:

providing a semiconductor die;

providing a leadframe having a die receiving area and a plurality of leads extending outwardly from positions adjacent the die receiving area, each of the leads having first and second portions and an intermediate portion, the first portion being closer to the die receiving area than the second portion, and the first and second portions being separated by the intermediate portion;

electrically coupling each first portion of the plurality of leads to the semiconductor die;

encapsulating the semiconductor die and portions of the plurality of leads with a resin encapsulating material to form a package body which completely contains the first portions, intermediate portions, and second portions of the leads such that a first surface of each of the second portions of the leads and an entire surface of the die receiving area are exposed on, and substantially flush with, one of either a top surface or a bottom surface of the package body; and

severing the plurality leads to create a second surface of each of the second portions of the leads which is exposed on, and substantially flush with, a side of the package to form the leadless semiconductor device in which only the first and second surfaces of the leads are exposed.

10. The method of claim **9** further comprising the step of attaching the semiconductor device to a substrate by soldering the exposed second portions of the leads on the bottom of the package body to the substrate.

11. A method for fabricating a leadless semiconductor device comprising the steps of:

providing a semiconductor die;

providing a leadframe having a plurality of leads, each of the leads having first and second portions and an intermediate portion, the first portions of the leads being used for electrical connection to the die, the second portions of the leads being used for electrical connection to the device, and the first and second portions being separated by the intermediate portion;

electrically coupling the first portions of each of the plurality of leads to the semiconductor die;

forming a package body from a resin encapsulating material, the package body completely containing the semiconductor die and the first, second, and intermediate portions of the plurality of leads such that a first surface of each of the second portions of the leads is exposed on, and substantially flush with, either a top surface or a bottom surface of the package body, such that a second surface of each second portion of the leads is exposed on, and substantially flush with a side of the package body, and such that only the first and second surfaces of the leads are exposed; and

plating the first and second exposed surfaces of the second portions of the leads with a conductive material.

12. The method of claim **11** wherein the step of plating the exposed areas of the second portions of the leads with a conductive material comprises plating the exposed areas of the second portions of the leads with solder.

* * * * *

UNITED STATES PATENT AND TRADEMARK OFFICE
CERTIFICATE OF CORRECTION

PATENT NO. : 5,172,214

DATED : December 15, 1992

INVENTOR(S) : James J. Casto

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

In claim 1, column 5, line 36:
after "package body" insert --wherein a second surface of each of the second portions of the leads is exposed on and substantially flush with the perimeter of the package body, and wherein only the first and second surfaces of the second portions of the leads are exposed--;

Cancel claim 2;

In claim 5, column 5, line 65:
after "second surfaces" insert --of the second portions--;

In claim 9, column 6, line 38:
after "second surfaces" insert --of the second portions--; and

In claim 11, column 6, line 67:
after "second surfaces" insert --of the second portions--.

On title page, "12 Claims, 1 Drawing Sheet" should read

--11 Claims, 1 Drawing Sheet--

Signed and Sealed this

Sixteenth Day of November, 1993

Attest:

BRUCE LEHMAN

Attesting Officer

Commissioner of Patents and Trademarks

[redacted]

EXHIBIT D

US005200362A

United States Patent [19]

Lin et al.

[11] Patent Number: 5,200,362

[45] Date of Patent: Apr. 6, 1993

[54] **METHOD OF ATTACHING CONDUCTIVE TRACES TO AN ENCAPSULATED SEMICONDUCTOR DIE USING A REMOVABLE TRANSFER FILM**

[75] Inventors: **Paul T. Lin; Michael B. McShane,** both of Austin, Tex.; **Sugio Uchida; Takehi Sato,** both of Nagano, Japan

[73] Assignee: **Motorola, Inc.,** Schaumburg, Ill.

[21] Appl. No.: **756,952**

[22] Filed: **Sep. 9, 1991**

Related U.S. Application Data

[63] Continuation of Ser. No. 576,255, Aug. 31, 1990, abandoned.

[30] **Foreign Application Priority Data**

Sep. 6, 1989 [JP] Japan 1-231323

[51] **Int. Cl.**[5] **H01L 21/56;** H01L 21/58; H01L 21/60

[52] **U.S. Cl.** **437/207;** 437/211

[58] **Field of Search** 437/206, 211, 220, 207; 264/272.17; 29/841, 855

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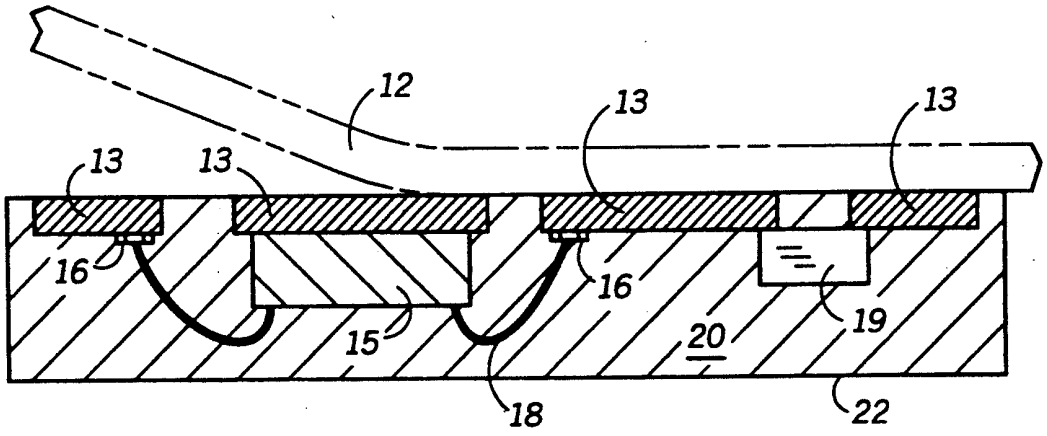
Primary Examiner—Olik Chaudhuri
Assistant Examiner—David E. Graybill
Attorney, Agent, or Firm—Jasper W. Dockrey

[57] **ABSTRACT**

A semiconductor device and a method for its fabrication are disclosed. In a preferred embodiment, a pattern of conductive traces is formed on a film of transfer material. A semiconductor device die is interconnected to the pattern of conductive traces and a resin body is formed around the die, one side of the conductive traces, and the interconnecting means. The film of transfer material forms, at this stage of the process, one side of the package. The film of transfer material is then peeled from the pattern of conductive traces and the resin body to expose the other side of the pattern of conductive traces. Contact to the other side of the pattern provides electrical contact to the senmiconductor device die.

8 Claims, 3 Drawing Sheets



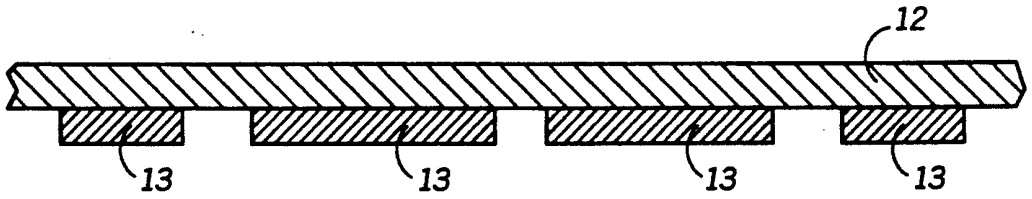


FIG.1

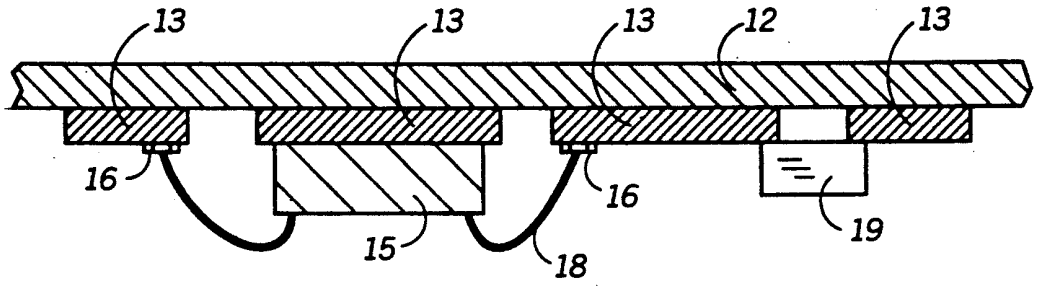


FIG.2

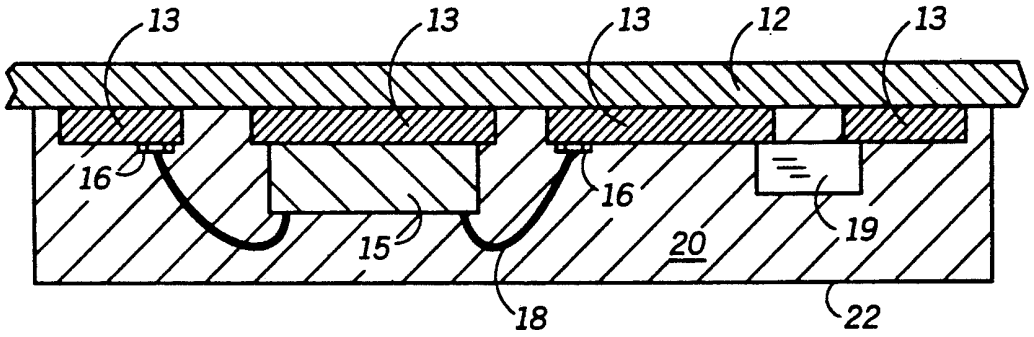


FIG.3

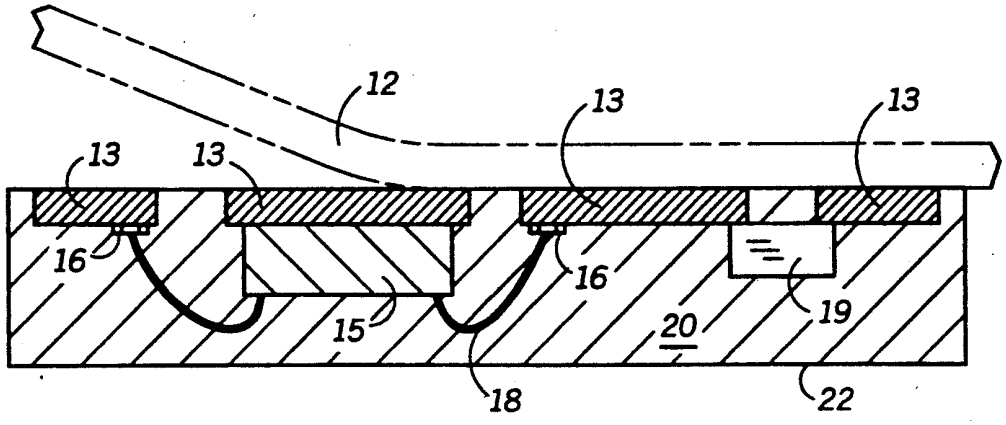


FIG.4

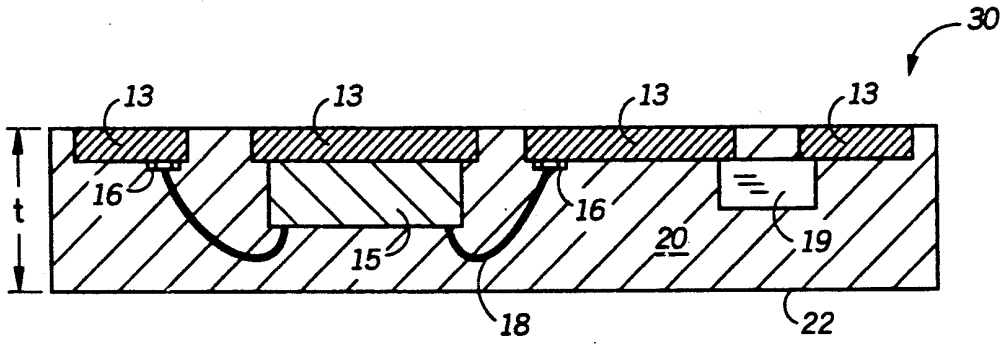


FIG. 5

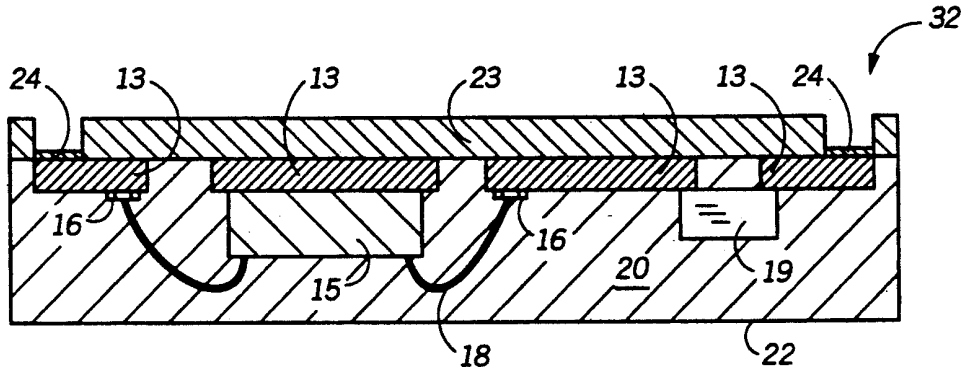


FIG. 6

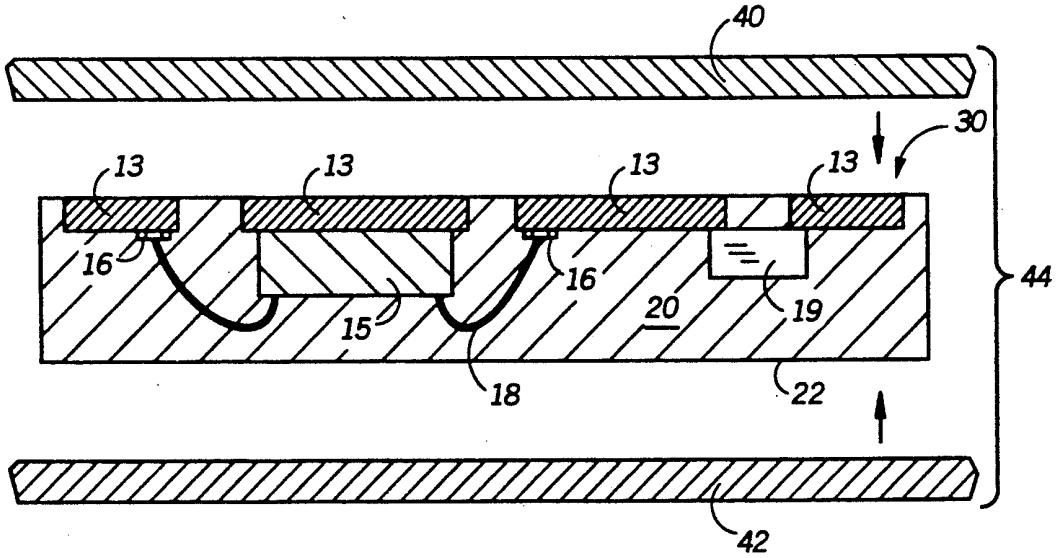


FIG. 7

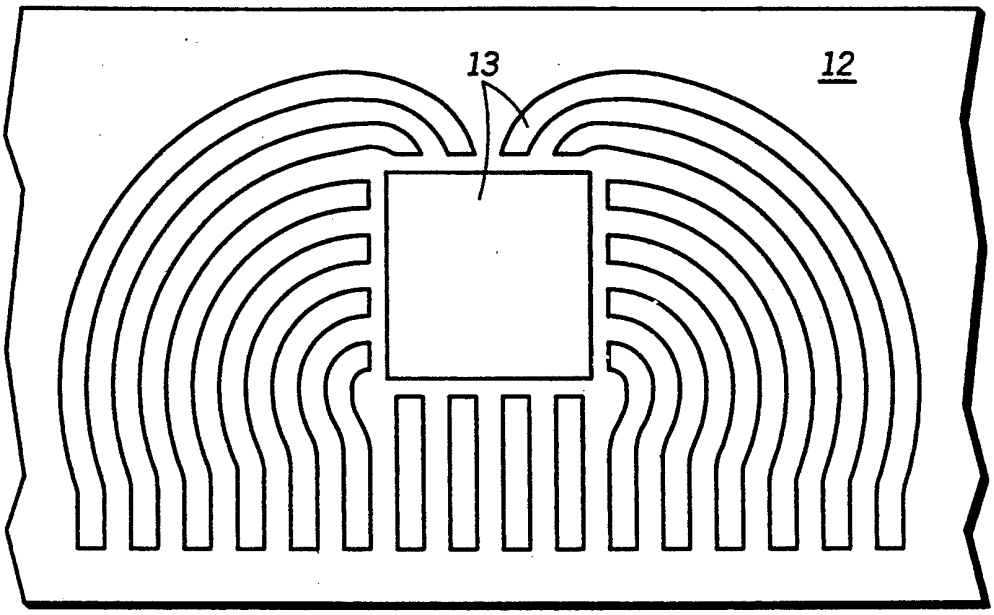


FIG.8

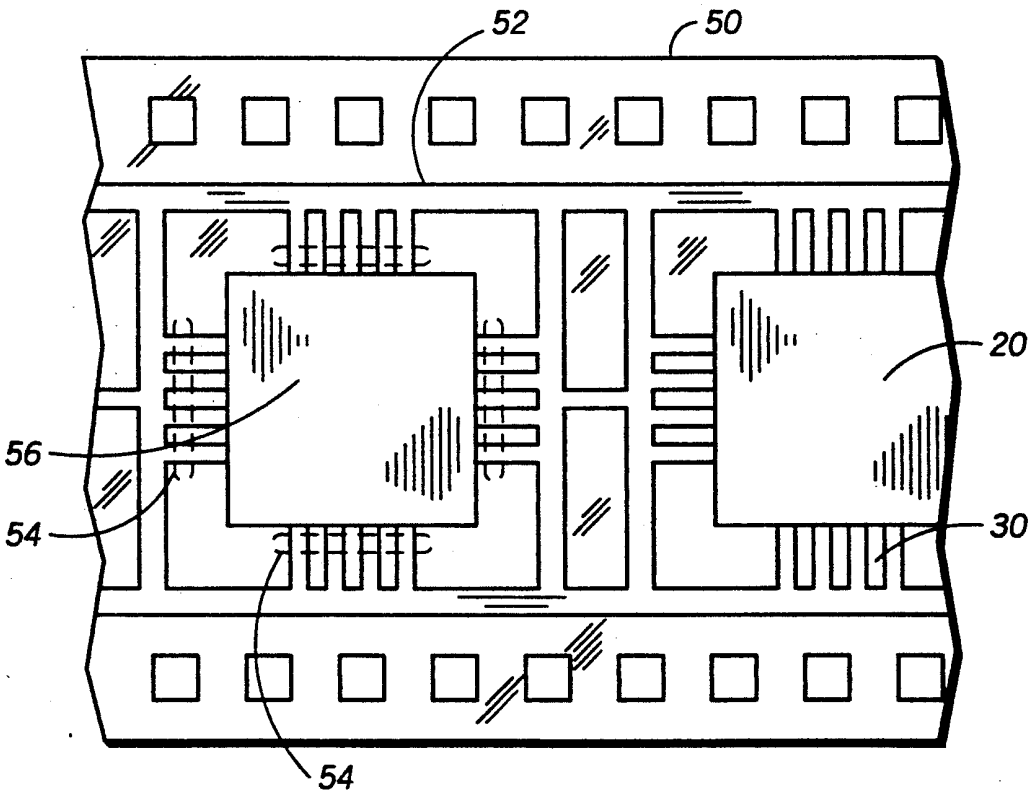


FIG.9

METHOD OF ATTACHING CONDUCTIVE TRACES TO AN ENCAPSULATED SEMICONDUCTOR DIE USING A REMOVABLE TRANSFER FILM

This is a continuation of application Ser. No. 07/576,255, filed Aug. 31, 1990, now abandoned.

BACKGROUND OF THE INVENTION

This invention relates to a resin encapsulated semiconductor device and to a method for its fabrication, and more specifically to a resin encapsulated semiconductor device capable of being fabricated in a thin format.

Semiconductor devices are widely used in various types of electronic products, consumer products, automobiles, integrated circuit cards, and the like. One feature of the semiconductor device which is important in many of these applications, and especially in such applications as the integrated circuit card, is the small size of the semiconductor device.

The semiconductor devices which are used in those various applications are usually packaged by either one of two methods. In one method, a semiconductor device die is placed in a package which is then individually mounted on a circuit substrate. In an alternate method, the semiconductor device die itself is mounted directly on the circuit substrate and then is usually provided with a protective encapsulation structure. The first mentioned method has the advantages that the device die is sealed in and protected by the package. The packaged device is easy to test, handle, and install and the encapsulating package provides the desired degree of protection against the environment. In contrast, the second described method in which the device die is connected directly to the substrate minimizes the area required by the die and thus allows a very high packing density. In this method, however, the device die is less easily handled and tested and is more subject to undesirable effects of the environment.

In selecting either of the above mentioned packaging techniques, it is necessary to compromise in the characteristics of the semiconductor device and the way it is utilized. In addition, either method requires that the semiconductor device be packaged on the interconnecting substrate such as a PC board, and thus has a problem of preventing the reduction in the thickness of the substrate so that the semiconductor device cannot be used in an application such as an IC card which requires an extremely thin substrate.

Thus a semiconductor device and a method for its fabrication were needed which would overcome the limitations of the foregoing semiconductor devices and methods.

BRIEF SUMMARY OF THE INVENTION

This invention provides a highly reliable packaged semiconductor device and a method for its fabrication which achieves a reduction in the thickness of the device without compromising the ease of handling a fully packaged device. In accordance with one embodiment of the invention, a semiconductor device is fabricated by providing a transfer film on which a pattern of conductive traces are provided. A semiconductor device die is interconnected to the pattern of conductive traces and a resin material is provided to encapsulate the semiconductor device die, one side of the pattern of conductive traces, and the electrical interconnections between the traces and the die. The transfer film is then peeled from the encapsulated device and the pattern of conductive traces to expose the underside of the pattern of traces, at least a portion of which is available for making electrical contact to the semiconductor device die.

BRIEF DESCRIPTION OF THE DRAWINGS

FIGS. **1–4** illustrate, in cross section, process steps in accordance with one embodiment of the invention for the fabrication of a semiconductor device;

FIGS. **5** and **6** illustrate, in cross section, semiconductor devices in accordance with two embodiments of the invention;

FIG. **7** illustrates schematically the fabrication of an integrated circuit (IC) card;

FIG. **8** illustrates a representative pattern of conductive traces on a transfer film; and FIG. **9** illustrates the fabrication of a plurality of semiconductor devices on an elongated transfer film in accordance with a further embodiment of the invention.

DETAILED DESCRIPTION OF PREFERRED EMBODIMENTS

FIGS. **1–4** illustrate, in cross section, process steps in accordance with one embodiment of the invention. As illustrated in FIG. **1**, a transfer film **12** is provided with a pattern of conductive traces **13** on one side of the film. A representative and illustrative pattern of such traces is shown in FIG. **8**. Transfer film **12** is a sheet film of flexible material such as "Kapton" or polyester upon which the pattern of conductive traces is formed.

The pattern of conductive traces can be formed in a number of different ways. In accordance with a preferred embodiment of the invention, a foil of conductive material such as copper is laminated to the transfer film **12** and is subsequently patterned using conventional photolithographic patterning and etching. Alternatively, the pattern of conductive traces can be formed, for example, by evaporating a layer of metal or other conductor onto the surface of the transfer film and then patterning that evaporated layer. If the evaporated layer is not of sufficient thickness to reduce the series resistance to a low enough value, the thickness can be increased by plating additional material onto the evaporated film. Still further, the pattern of conductive traces can be formed by first applying a reverse photoresist mask to the transfer film, evaporating a conductive material onto the photoresist and the transfer film, and then using a lift off process to remove the unwanted conductive material. In yet another embodiment, a pattern of traces is formed from a thin sheet of metal and that pattern of traces is then laminated to the transfer film.

A semiconductor device die **15** is electrically interconnected to the pattern of conductive traces. The interconnection is accomplished by wirebonds **18** or by other conventional means such as TAB tape, or the like. The semiconductor die can be affixed to a portion of the pattern of conductive traces, for example by solder, conductive epoxy, or the like or can be attached to the pattern only by the interconnecting means **18**. If the die is attached to a portion of the pattern of conductive traces, that portion can be used, if necessary, as an electrical contact to a substrate of the semiconductor device die. As also illustrated in FIG. **2**, additional circuit elements **19** can also be attached to and interconnected with the pattern of conductive traces. Circuit element

19 can be, for example, a resistor, diode, capacitor, or the like. The additional circuit element, which can also be an additional semiconductor device die, can be connected between traces, as illustrated, or can be bonded to the conductive traces as is device die 15.

The portion 16 of the pattern of conductive traces to which the wirebonds or other interconnecting means are joined can be prepared especially to accommodate the attachment of the interconnecting means. For example, the bonding area 16 can be plated with gold, treated to smooth the area, or otherwise treated to enhance the reliability of the interconnection.

As illustrated in FIG. 3, the process continues by the encapsulation of the semiconductor device die 15, additional circuit element 19, interconnecting means 18, and one side of the pattern of conductive traces by an encapsulating resin 20 to form a protective body 22. Body 22 is formed in conventional manner, such as by transfer molding in which the transfer film 12 with the attached semiconductor device die 15 is inserted into a mold cavity and the encapsulating resin is forced into the cavity at a high temperature and high pressure. Alternatively, body 22 can be made by injection molding, pour molding, or in a "glop top" process. In each of these encapsulating operations, the resin material is formed on one side of transfer film 12; that is, the transfer film, at this stage of the process, forms one side of the package. The resin material thus surrounds the semiconductor device die, the interconnecting means, and one side of the pattern of conductive traces, plus any additional electronic components which are attached to the conductive traces.

Following the encapsulation operation, as illustrated in FIG. 4, the transfer film 12 is peeled or removed from the surface of the encapsulated device leaving a resin encapsulated device with one side of the conductive traces exposed and available to provide electrical contact to the semiconductor device die. In forming the pattern of conductive traces on transfer film 12, for example by applying a layer of electrolytic copper foil to the transfer film, it is especially advantageous if the surface of the foil which is to contact the transfer film is smooth and the opposite side is rough. The smooth surface facilitates the peeling away of the transfer film after the encapsulation operation and the rough surface enhances the adherence of the resin material to the pattern of conductive traces.

FIG. 5 illustrates, again in cross section, the completed semiconductor device 30 after the transfer film has been removed. Device 30 includes semiconductor device die 15 which is enclosed within an encapsulating resin body 22. Exposed on one side of the resin body are portions of one side of the pattern of conductive traces 13. These conductive traces can be directly contacted for making electrical contact to the semiconductor device die. No thick device "header" or leadframe is necessary for mounting the device die, and so the thickness "t" is minimized. In addition to making contact to the conductive traces for the purpose of making electrical contact, some of the traces, such as trace 13 upon which device die 15 is mounted, can be contacted by a heat sink (not shown) in order to conduct heat away form the die during operation.

FIG. 6 illustrates, in cross section, a semiconductor device 32 in accordance with an alternate embodiment of the invention. This embodiment is similar to device 30 illustrated in FIG. 5 except that a protective coating 23 is applied to the exposed surface of the pattern of conductive traces 13. The protective coating can be, for example, a low temperature deposited oxide, polyimide, adhesively applied insulating film, or the like. Openings 24 are formed through insulating film 23 to expose selected portions of the pattern of conductive traces. Gold plating or other metallic plating can be applied to the exposed portions of the conductive traces to protect against corrosion of the those exposed portions and also to enhance the ability to electrically contact those portions. In device 32 only the contacts 24 are exposed and the rest of the semiconductor device is encapsulated either by encapsulating body 22 or by the protective film 23.

FIG. 7 illustrates schematically, in exploded view, a further embodiment of the invention. As illustrated in FIG. 7, an IC card structure or the like is fabricated by laminating a device such as device 30 between upper 40 and lower 42 plastic sheets. The three components are laminated together to form an IC card device 44. The term "IC card" is used to describe the debit cards and the like which incorporate an integrated circuit to update the financial or other status of the card as money is deposited or as the card is used. IC device 30 provides the intelligence included within the IC card. The flat plastic sheets 40, 42 provide a useful card size and include identifying information embossed on the faces as well as other information and user interface. The underside of sheet 40 may include a pattern of traces which interface with the pattern of traces 13 on device 30. The traces may be coupled together with solder bumps, conductive epoxy, or the like, or merely by the pressure of the lamination itself. Electrical contacts on the edge of one of the plastic sheets then provides an external electrical access to the device 30. Alternatively, device 30 itself, with a pattern as that illustrated in FIG. 5, may directly provide the external contact. For example, sheet 40 may be provided with a window or windows (not shown) which expose the pattern of traces on device 30 so that contact, for example by a card reader machine, can be made directly to those traces.

FIG. 9 illustrates, in plan view, the fabrication of semiconductor devices in accordance with a further embodiment of the invention in which a plurality of devices can be fabricated simultaneously. An elongated transfer film 50 provides a plurality of groups of patterns of conductive traces (parts of two groups are illustrated) on one surface thereof. The conductive traces are interconnected by a bus line 52 which allows the plurality of traces to be electrolytically plated. The patterns of conductive traces can be made, for example, by evaporating a film of conductive material onto the surface of elongated transfer film 50, patterning that evaporated film into the desired pattern, and then electroplating to achieve the desired thickness of conductive material. A semiconductor device die is mounted and interconnected to each of the groups of conductive traces and the die, interconnections, and one side of the conductive traces are encapsulated within a resin body 56. After the resin encapsulation, which is carried out in a manner similar to that described above, the elongated transfer film is peeled off or otherwise removed to expose the reverse side of the conductive traces. Either before or after the transfer film is removed, the traces can be severed along the lines 54 to electrically disconnect the individual devices so that they can be tested.

Thus it is apparent that there has been provided, in accordance with the invention, a semiconductor device and method for its fabrication which overcomes the

problems associated with the prior art devices and methods. Although the invention has been described and illustrated with reference to specific embodiments thereof, it is not intended that the invention be limited to these illustrative embodiments. Those skilled in the art will recognize that variations and modifications can be made without departing from the spirit of the invention. For example, other patterns of conductive traces can be used and additional devices can be interconnected as needed. Additionally, other methods for forming both the conductive traces and for the encapsulation of the devices are possible. Thus it is intended to encompass within the invention all such variations and modifications as fall within the scope of the appended claims.

We claim:

1. A process for fabricating a semiconductor device comprising the steps of:

providing a transfer film;

providing a pattern of conductive traces on said transfer film;

providing a semiconductor device die;

forming electrical interconnections between said pattern of conductive traces and said semiconductor device die;

providing a resin material on one side of said transfer film to encapsulate said semiconductor device die, said electrical interconnections, and a portion of said pattern of conductive traces; and

removing said transfer film to expose one side of said pattern of conductive traces.

2. The process of claim 1 further comprising the step of forming a layer of insulating material over portions of said one side and leaving contact areas of said pattern exposed.

3. The process of claim 1 further comprising the step of laminating said semiconductor device die and said resin material between two sheets of plastic material.

4. The process of claim 3 wherein said step of laminating leaves exposed a portion of said one side.

5. The process of claim 4 further comprising the step of plating contact metal onto said exposed portion.

6. The process of claim 1 wherein said step of forming a pattern of conductive traces comprises the steps of:

forming a continuous layer of conductive material on said transfer film; and

selectively etching said continuous layer to form said pattern of conductive traces.

7. The process of claim 6 wherein said step of forming a continuous layer comprises laminating a layer of conductive foil to said transfer film.

8. The process of claim 6 wherein said step of forming a continuous layer comprises evaporating a layer of metal onto said transfer film.

* * * * *

EXHIBIT E

US005434739A

United States Patent [19]

Heck

[11] Patent Number: 5,434,739

[45] Date of Patent: Jul. 18, 1995

[54] **REVERSE BATTERY PROTECTION CIRCUIT**

[75] Inventor: **Karl R. Heck**, Phoenix, Ariz.

[73] Assignee: **Motorola, Inc.**, Schaumburg, Ill.

[21] Appl. No.: **75,839**

[22] Filed: **Jun. 14, 1993**

[51] **Int. Cl.**[6] **H02H 3/18**

[52] **U.S. Cl.** **361/84**; 361/56

[58] **Field of Search** 361/84, 85, 92, 90, 361/56, 91, 77

[56] **References Cited**

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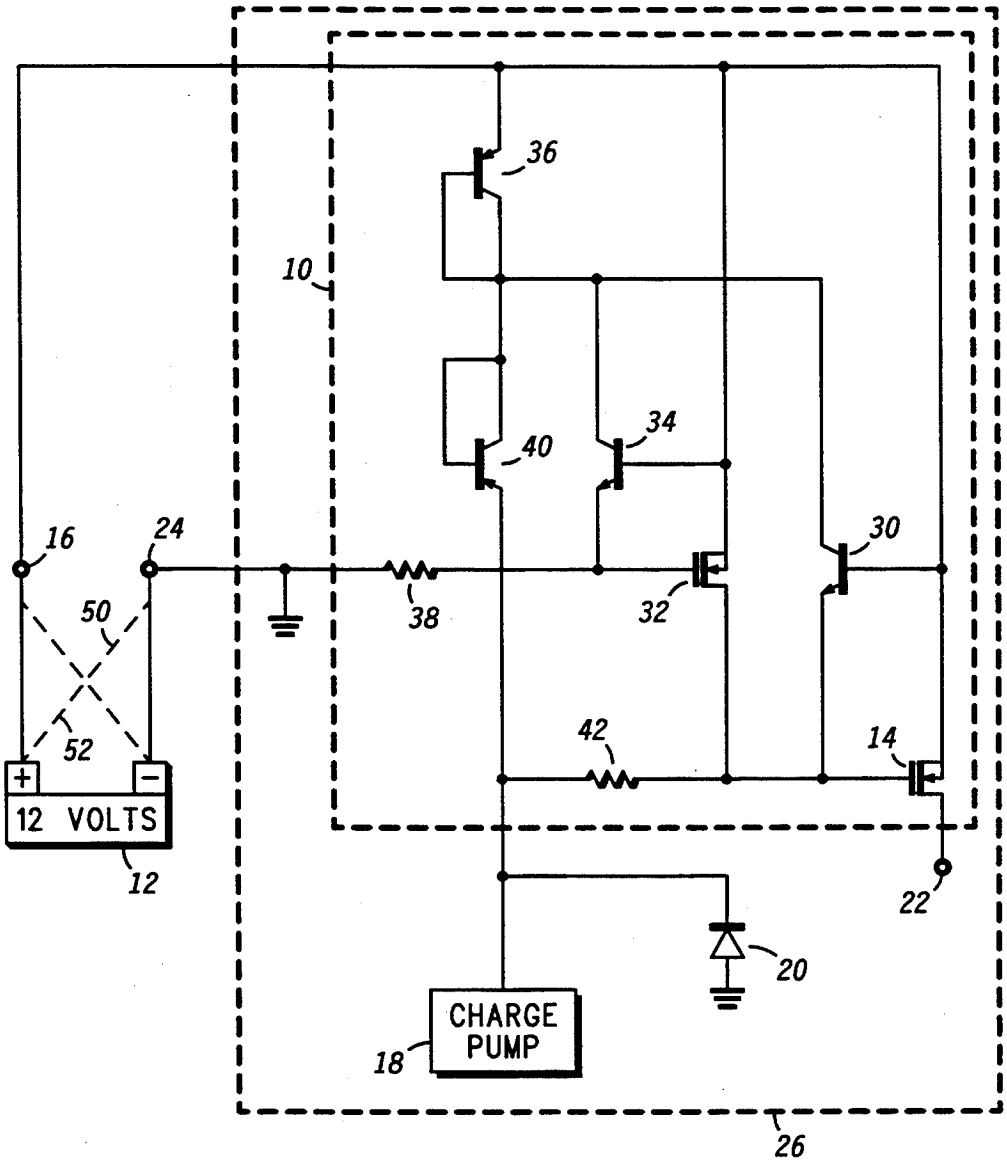
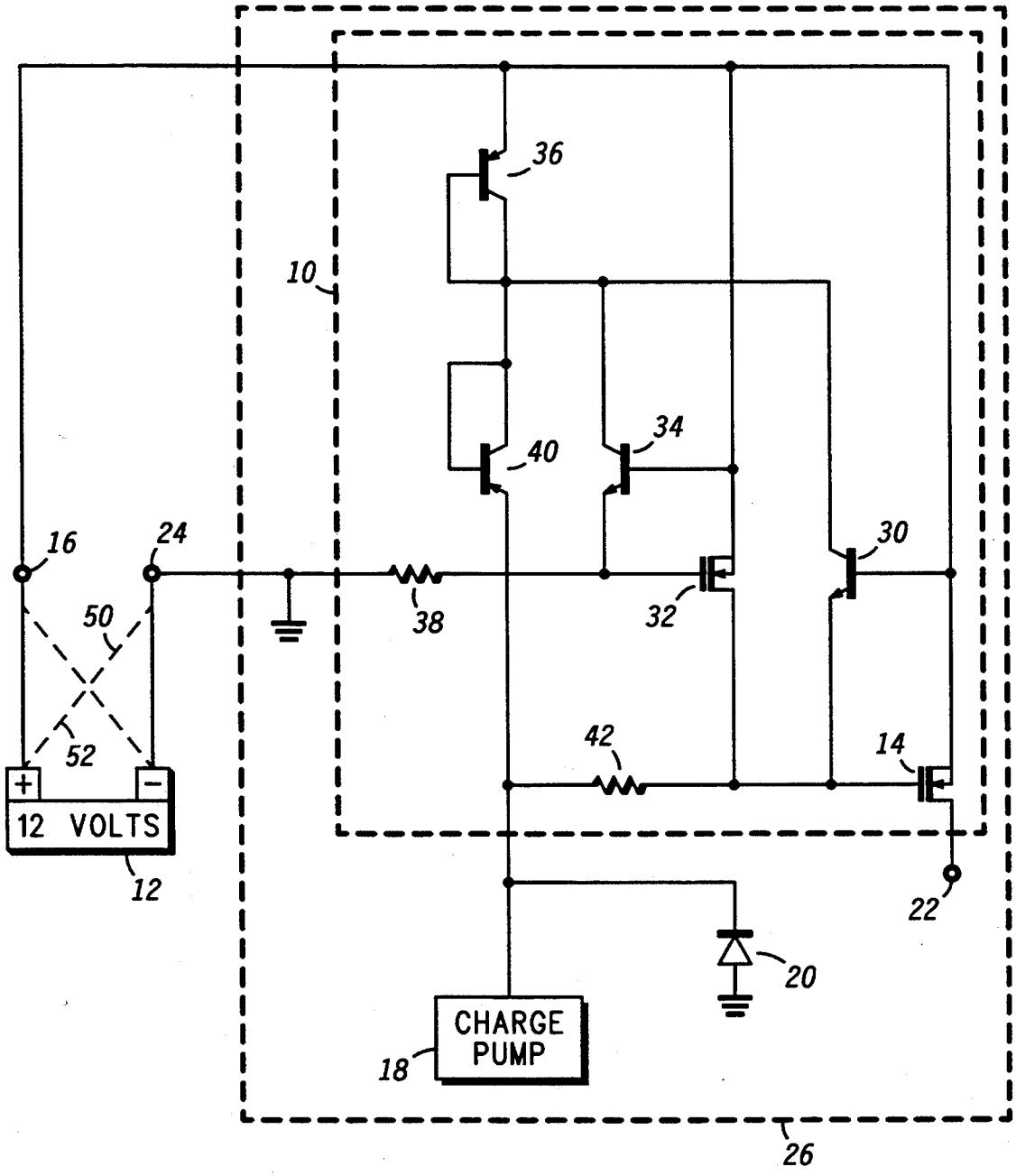
Primary Examiner—Marc S. Hoff
Assistant Examiner—S. Jackson
Attorney, Agent, or Firm—Rennie William Dover

[57] **ABSTRACT**

A protection circuit (**10**) for protecting internal circuitry of an integrated circuit (**26**) from a reverse battery connection has been provided. The protection circuit includes a pass transistor (**14**) which is rendered operative when the supply voltage is properly connected to the integrated circuit. However, when the power supply is improperly connected, a second transistor (**32**) becomes active thereby rendering the pass transistor inactive and not allowing the reverse supply voltage to be applied to the internal circuitry.

8 Claims, 1 Drawing Sheet




36
10
40
34
16
24
30
50
38
32
52
42
14
12 VOLTS
12
22
20
CHARGE PUMP
18
26

REVERSE BATTERY PROTECTION CIRCUIT

FIELD OF THE INVENTION

This invention relates to protection circuits and, in particular but not limited to, a reverse battery protection circuit for use in automotive applications.

BACKGROUND OF THE INVENTION

There currently exists a numerous types of electronic integrated circuits (IC's) for use in the automotive industry. Generally, the power supply for these circuits are generated from a 12-volt battery in an automobile. However, automotive IC's tied to the battery must survive the battery being hooked up backwards, for example, to avoid forward biasing epitaxial layers of the IC that are tied to the battery which thereby could result in destruction of the IC.

One attempt that prior art has made for providing reverse battery protection for IC's is to include a series diode between the battery and the integrated circuit wherein if the integrated circuit is connected to the battery backwards, the series diode is reversed biased and prevents supply voltage from being applied to the integrated circuit. However, the series diode solution compromises low voltage performance and the geometry of the diode becomes larger as supply current requirements increase.

Another attempt that prior art has made in providing reverse battery protection for an integrated circuit is to provide a saturated lateral PNP transistor in series between the battery and the integrated circuit. Although low voltage performance is not compromised in this solution, base current requirements for the lateral PNP increase power dissipation and the geometry of the PNP transistor becomes large as supply current requirements increase.

Another attempt that prior art has made in providing reverse battery protection for an integrated circuit is to provide a charged pumped reverse TMOS transistor as a pass device between the battery and the integrated circuit wherein the TMOS transistor has passive (resistive) gate to source termination. However, this solution requires DC current from the charge pump to enhance the TMOS transistor, and the turn off time of the TMOS transistor is limited by the size of the passive gate termination. Moreover, the charge pump must be high impedance when the supply voltage is reversed.

Hence, there exists a need for an improved reverse battery protection circuit for an integrated circuit that does not compromise low voltage performance, can efficiently handle moderate supply currents, does not demand DC current from a charge pump, and has a fast turn off time.

BRIEF DESCRIPTION OF THE DRAWING

The sole figure illustrates a detailed schematic diagram of a reverse battery protection circuit for protecting an integrated circuit in accordance with the present invention.

DETAILED DESCRIPTION OF THE DRAWING

Referring to the sole figure, there is illustrated reverse battery protection circuit **10** fabricated within integrated circuit (IC) **26** and being coupled between battery **12** and terminal **22**. It is understood that terminal **22** is further coupled to additional circuitry wherein this additional circuitry is desired to be protected from

reverse battery hook up. IC **26** includes protection circuit **10** as well as charge pump **18**, and any additional circuitry (not shown) coupled to terminal **22**. Terminal **24** is coupled to a ground reference of IC **26**.

Protection circuit **10** includes pass transistor **14** having a source electrode coupled to terminal **16** while the gate electrode of transistor **14** is coupled through resistor **42** to charge pump **18**. The back gate of transistor **14** is coupled to the source electrode of transistor **14** while the drain electrode of transistor **14** is coupled to terminal **22**.

Protection circuit **10** further includes transistor/zener diode **30** having a base coupled to terminal **16** and an emitter coupled to the gate electrode of transistor **14** and to the drain electrode of transistor **32**. The collector of transistor **30** is coupled to the collectors of transistor/zener diode **34** and transistor/diode **36** wherein the collector of transistor **36** is coupled to its base. The emitter of transistor **36** and the base of transistor **34** are both coupled to terminal **16**.

Moreover, the source electrode of transistor **32** and the back gate electrode of transistor **32** are coupled to terminal **16**. The emitter of transistor **34** is coupled to the gate electrode of transistor **32** and returned to ground through resistor **38**. The collector of transistor **34** is coupled to the collector of transistor/diode **40** wherein transistor **40** has its base coupled to its collector. The emitter of transistor **40** is coupled through resistor **42** to the gate electrode of transistor **14**. Moreover, the emitter of transistor **40** is coupled to charge pump **18**.

Charge pump **18** is coupled through diode **20** and returned to ground reference. In normal operation, transistor **14** requires the use of charge pump **18** to generate a voltage of at least 5 volts above a voltage supplied by battery **12**. Moreover, charge pump **18** is typically available on IC **26** since it is required for other applications.

Under proper connection, the positive terminal of battery **12** is coupled to terminal **16** while the negative terminal of battery **12** is coupled to terminal **24**. As a result, a positive supply voltage is applied to the source electrodes of transistors **32** and **14** as is desired. In this situation, transistor **14** is rendered operative while transistor **32** is rendered non-operative. As a result, the voltage appearing at terminal **22** (with respect to ground reference) will be substantially equal to the voltage appearing at terminal **16** (with respect to ground reference) less any IR drop occurring across transistor **14**.

However, if battery **12** is improperly hooked up in a reverse manner wherein the positive terminal of battery **12** is coupled to terminal **24** while the negative terminal of battery **12** is coupled to terminal **16** as represented by dotted lines **50** and **52**. This now means that a negative voltage (with respect to ground reference) is applied to the source electrodes of transistors **14** and **32** as is not desired. Under this condition, transistor **32** is rendered operative thereby shorting the gate electrode of transistor **14** to its source electrode and, thus, rendering transistor **14** non-operative. As a result, the voltage appearing at terminal **16** is not passed to terminal **22** and thus is not supplied to any additional internal IC circuitry. Further, any epitaxial layers typically coupled to terminal **22** cannot conduct current and damage integrated circuit **26**.

Transistor **30** functions as a zener diode to protect excessive voltage from appearing on the gate electrode of transistor **14**. Essentially, the base of transistor **30** is the anode of the zener diode while the emitter of transistor **30** is the cathode of the zener diode. Moreover, the collector of transistor **30** is the third terminal of the zener diode and is coupled to the collector of transistor **34** which is the epitaxial island. Similarly, transistor **34** functions as a zener diode to protect excessive voltage from appearing on the gate electrode of transistor **32** wherein the base and emitters of transistor **34** respectively act as the anode and cathode of the zener diode while the collector of transistor **34** is coupled to the epitaxial island.

Moreover, resistor **38** functions to provide charge to render transistor **32** operative under a reverse battery condition. Also, resistor **42** functions to decouple the gate electrode of transistor **14** from charge pump **18**.

It should be noted that components **30**, **34**, **32** and **38** are all fabricated in one epitaxial region which is biased by PNP transistors **36** and **40**.

The present invention assures that no epitaxial islands are tied to terminal **16**. As a result, if the connections of battery **12** are reversed, there are not epitaxial islands to be forward biased.

The present invention has several advantages. First, protection circuit **10** does not provide any additional DC loading on charge pump **18** when it is desired to enhance and turn on TMOS transistor **14**. Second, under reverse battery conditions, charge pump **18** does not have to be heavily resistive or open for proper operation as is the case for prior art circuits. Thus, charge pump **18** does not have any special design requirements. Third, protection circuit **10** provides reverse battery protection without sacrificing power supply head room for low voltage operation since no series diodes are used. Moreover, the present invention quickly renders transistor **14** non-operative under a reverse battery condition. In particular, the discharge time constant for the gate electrode of transistor **14** is a product of the drain-source on resistance (R_{DSON}) of transistor **32** and the input capacitance (C_{ISS}) of transistor **14** which is substantially less than the turn off time for a passive gate termination scheme.

By now it should be apparent from the foregoing discussion that a novel protection circuit for protecting internal circuitry of an integrated circuit from a reverse battery connection has been provided. The protection circuit includes a pass transistor which is rendered operative when the supply voltage is properly connected to the integrated circuit. However, when the power supply is improperly connected, a second transistor becomes active thereby rendering the pass transistor inactive and not allowing the reverse supply voltage to be applied to the internal circuitry.

While the invention has been described in specific embodiments thereof, it is evident that many alterations, modifications and variations will be apparent to those skilled in the art. Further, it is intended to embrace all such alterations, modifications and variations in the appended claims.

I claim:

1. An integrated circuit having reverse battery protection, the integrated circuit including a charge pump and internal circuitry, the integrated circuit also including a protection circuit coupled between a first and second terminals wherein the first terminal is coupled to a battery and the second terminal is coupled to the internal circuitry, the protection circuit comprising:

a pass transistor having first and second current carrying electrodes and a control electrode, said first and second current carrying electrodes of said pass transistor respectively coupled between the first and second terminals, said control electrode of said pass transistor coupled to the charge pump;

a first transistor (**32**) having first and second current carrying electrodes and a control electrode, said first current carrying electrode of said first transistor coupled to said control electrode of said pass transistor, said second current carrying electrode of said first transistor coupled to the first terminal;

a second transistor (**30**) having a collector, a base and an emitter, said base of said second transistor being coupled to the first terminal, said emitter of said second transistor coupled to said first current carrying electrode of said first transistor;

a third transistor (**34**) having a collector, a base and an emitter, said base of said third transistor coupled to the first terminal, said emitter of said third transistor coupled to said control electrode of said first transistor, said collector of said third transistor coupled to said collector of said second transistor;

a fourth transistor (**40**) having a collector, a base and an emitter, said collector of said fourth transistor coupled to said collector of said third transistor, said base of said fourth transistor coupled to said collector of said fourth transistor, said emitter of said fourth transistor coupled to said control electrode of said pass transistor;

a fifth transistor (**36**) having a collector, a base and an emitter, said collector of said fifth transistor coupled to said collector of said fourth transistor, said base of said fifth transistor coupled to said collector of said fifth transistor, said emitter of said fifth transistor coupled to the first terminal; and

a first resistor (**38**) coupled between said control electrode of said first transistor and a first supply voltage terminal.

2. The protection circuit according to claim **1** further including a second resistor (**42**) coupled between said emitter of said fourth transistor and said control electrode of said pass transistor.

3. A circuit for protecting internal circuitry of an integrated circuit from reverse battery connection, the integrated circuit including a charge pump and having first and second terminals coupled to a battery for supplying power to the integrated circuit, the circuit comprising:

first means for passing a voltage appearing across the first and second terminals to the internal circuitry when the integrated circuit is properly connected to the battery, said first means coupled between the first terminal and the integrated circuit and coupled to the charge pump;

second means for rendering said first means non-operative when the integrated circuit is improperly connected to the battery thereby blocking said voltage appearing across said first and second terminals from being passed to the internal circuitry, said second means including a first transistor which is rendered operative when the integrated circuit is improperly connected to the battery, said second means coupled between the first terminal and said first means.

4. The circuit according to claim 3 wherein said second means includes:

said first transistor (32) having first and second current carrying electrodes and a control electrode, said first current carrying electrode of said first transistor coupled to said first means, said second current carrying electrode of said first transistor coupled to the first terminal;

a second transistor (30) having a collector, a base and an emitter, said base of said second transistor coupled to the first terminal, said emitter of said second transistor coupled to said first current carrying electrode of said first transistor;

a third transistor (34) having a collector, a base and an emitter, said base of said third transistor coupled to the first terminal, said emitter of said third transistor coupled to said control electrode of said first transistor, said collector of said third transistor coupled to said collector of said second transistor;

a fourth transistor (40) having a collector, a base and an emitter, said collector of said fourth transistor coupled to said collector of said third transistor, said base of said fourth transistor coupled to said collector of said fourth transistor;

a fifth transistor (36) having a collector, a base and an emitter, said collector of said fifth transistor coupled to said collector of said fourth transistor, said base of said fifth transistor coupled to said collector of said fifth transistor, said emitter of said fifth transistor coupled to the first terminal;

a first resistor (38) coupled between said control electrode of said first transistor and a first supply voltage terminal; and

a second resistor (42) coupled between said emitter of said fourth transistor and said first means.

5. The circuit according to claim 3 wherein said second means includes:

a first transistor (32) having first and second current carrying electrodes and a control electrode, said first current carrying electrode of said first transistor coupled to said first means, said second current carrying electrode of said first transistor coupled to the first terminal;

first zener diode means (30) coupled across said second and control electrodes of said first transistor for limiting a voltage appearing thereacross; and

bias means coupled between the first terminal and said first means for biasing an epitaxial region in which said first transistor and said first zener diode means are fabricated.

6. The circuit according to claim 5 wherein said second means further includes second zener diode means (34) coupled across said first means for limiting a voltage appearing thereacross, said second zener diode means also being fabricated in said epitaxial region.

7. A method for providing reverse battery protection to internal circuitry of an integrated circuit, the integrated circuit having first and second terminals for coupling to a battery, the method comprising the steps of:

allowing a voltage appearing at the first terminal to pass through a transistor to the internal circuitry when the integrated circuit is properly coupled to the battery; and

actively disabling said transistor when the integrated circuit is improperly coupled to the battery thereby preventing said voltage appearing at the first terminal to pass to the internal circuitry.

8. An integrated circuit having reverse battery protection, the integrated circuit including a charge pump and internal circuitry, the integrated circuit also including a protection circuit coupled between first and second terminals wherein the first terminal is coupled to a battery and the second terminal is coupled to the internal circuitry, the protection circuit comprising:

a pass transistor having first and second current carrying electrodes and a control electrode, said first and second current carrying electrodes of said pass transistor respectively coupled between the first and second terminals, said control electrode of said pass transistor coupled to the charge pump; and

a first transistor for actively disabling said pass transistor when the battery is improperly connected thereby preventing a voltage appearing on the first terminal from appearing at the second terminal, said first transistor having first and second current carrying electrodes and a control electrode, said first current carrying electrode of said first transistor coupled to said control electrode of said pass transistor, said second current carrying electrode of said first transistor coupled to said first current carrying electrode of said pass transistor, said control electrode of said first transistor coupled to ground reference.

* * * * *

EXHIBIT F

US005476816A

United States Patent [19]

Mautz et al.

[11] **Patent Number: 5,476,816**

[45] **Date of Patent: Dec. 19, 1995**

[54] **PROCESS FOR ETCHING AN INSULATING LAYER AFTER A METAL ETCHING STEP**

[75] Inventors: **Karl E. Mautz**, Austin; **Jeffrey G. Cadenhead**, Kyle; **Thomas M. Allen**; **H. Adam Stevens**, both of Austin, all of Tex.

[73] Assignee: **Motorola, Inc.**, Schaumburg, Ill.

[21] Appl. No.: **219,123**

[22] Filed: **Mar. 28, 1994**

[51] **Int. Cl.**[6] **H01L 21/44**

[52] **U.S. Cl.** **437/195**; 437/235; 156/653.1

[58] **Field of Search** 437/195, 235; 156/653.1; 148/DIG. 51

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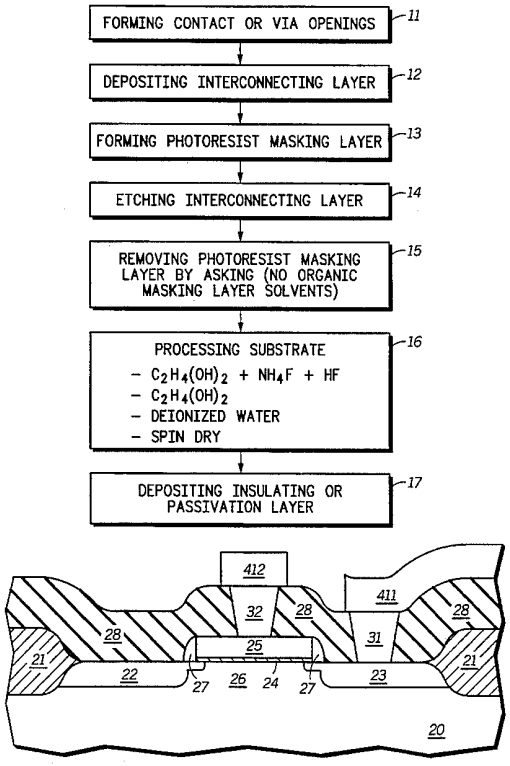
Primary Examiner—George Fourson
Assistant Examiner—C. Everhart
Attorney, Agent, or Firm—George R. Meyer

[57] **ABSTRACT**

A metal etch processing sequence eliminates the need to use an organic masking layer solvent and etches a portion of an insulating layer after a plasma metal etching step. The etch of the insulating layer is performed with an etching solution that may include 1,2-ethanediol, hydrogen fluoride, and ammonium fluoride. The etching solution etches in a range of 100–900 angstroms of the insulating layer. The etch removes at least 75 percent of the mobile ions within the insulating layer, and should remove at least 95 percent of the mobile ions. The process may be implemented using an acid hood, an acid compatible spray tool, or a puddle processing tool. The process includes many different embodiments that allow the process to be easily integrated into many different existing processing sequences. A similar process may be used with a resist-etch-back processing sequence.

21 Claims, 5 Drawing Sheets



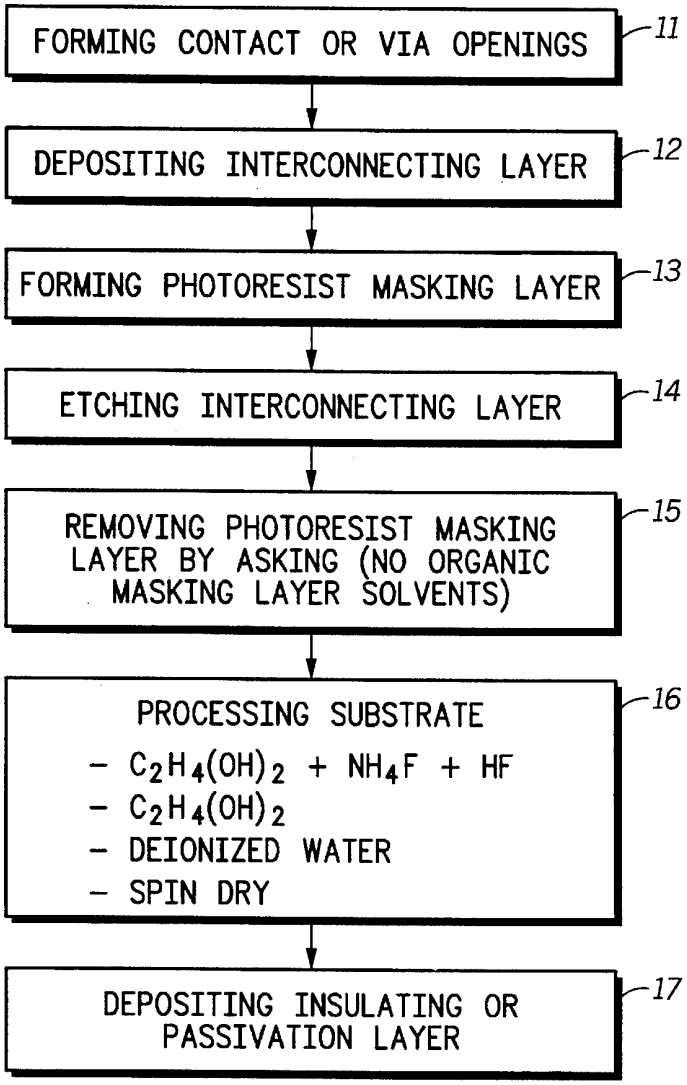

FORMING CONTACT OR VIA OPENINGS
11
DEPOSITING INTERCONNECTING LAYER
12
FORMING PHOTORESIST MASKING LAYER
13
ETCHING INTERCONNECTING LAYER
14
REMOVING PHOTORESIST MASKING LAYER BY ASKING (NO ORGANIC MASKING LAYER SOLVENTS)
15
PROCESSING SUBSTRATE
- $C_2H_4(OH)_2$ + NH_4F + HF
- $C_2H_4(OH)_2$
- DEIONIZED WATER
- SPIN DRY
16
DEPOSITING INSULATING OR PASSIVATION LAYER
17

FIG.1

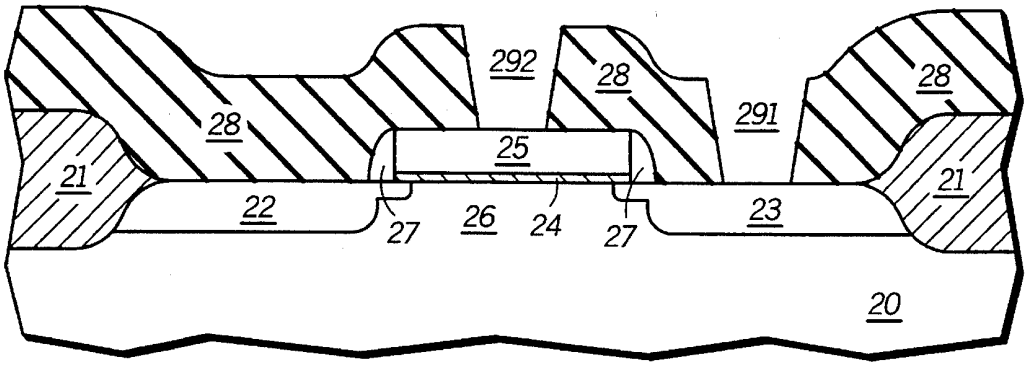

292
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FIG.2

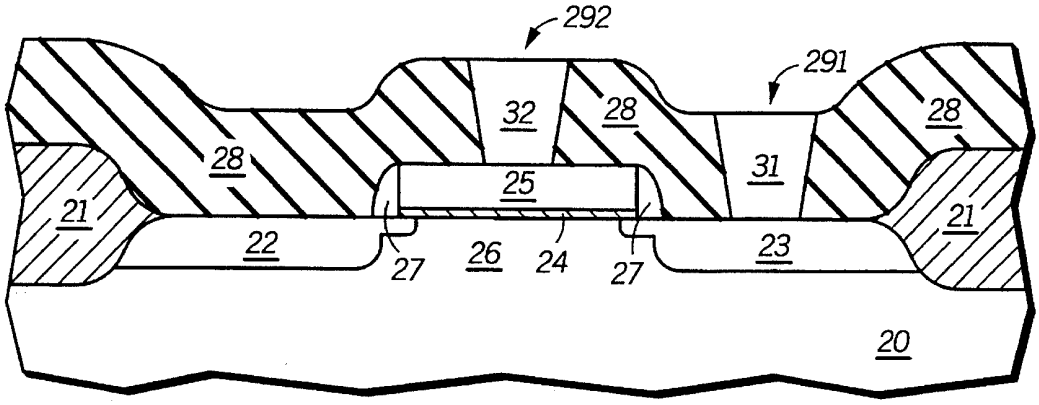

FIG.3

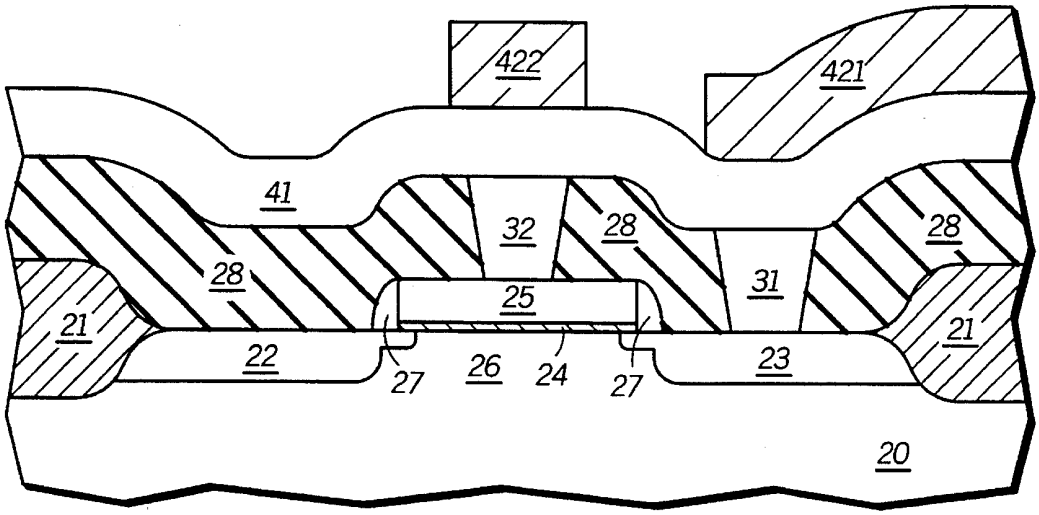

FIG.4

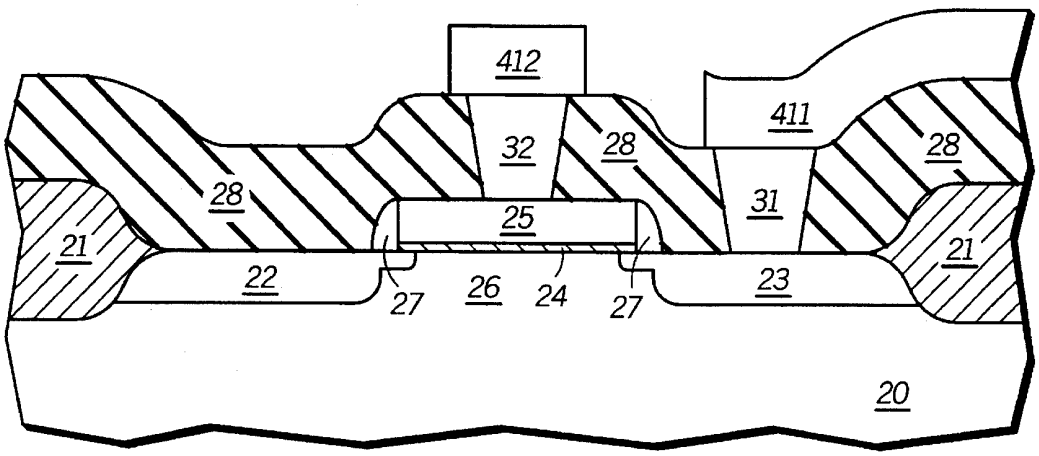

FIG.5

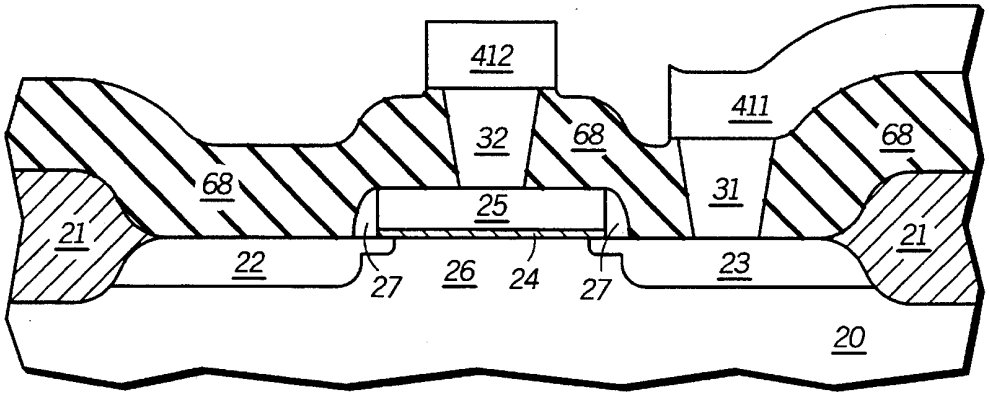

FIG.6

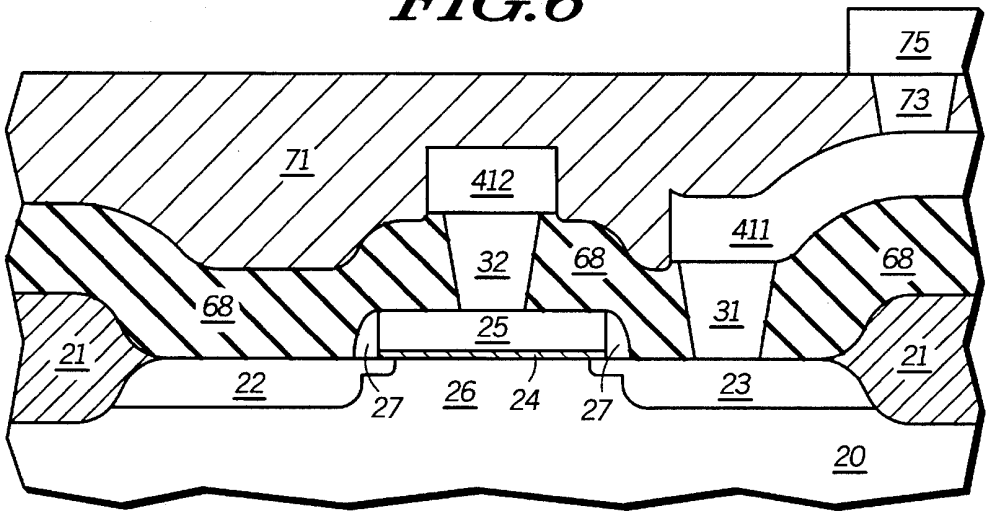

FIG.7

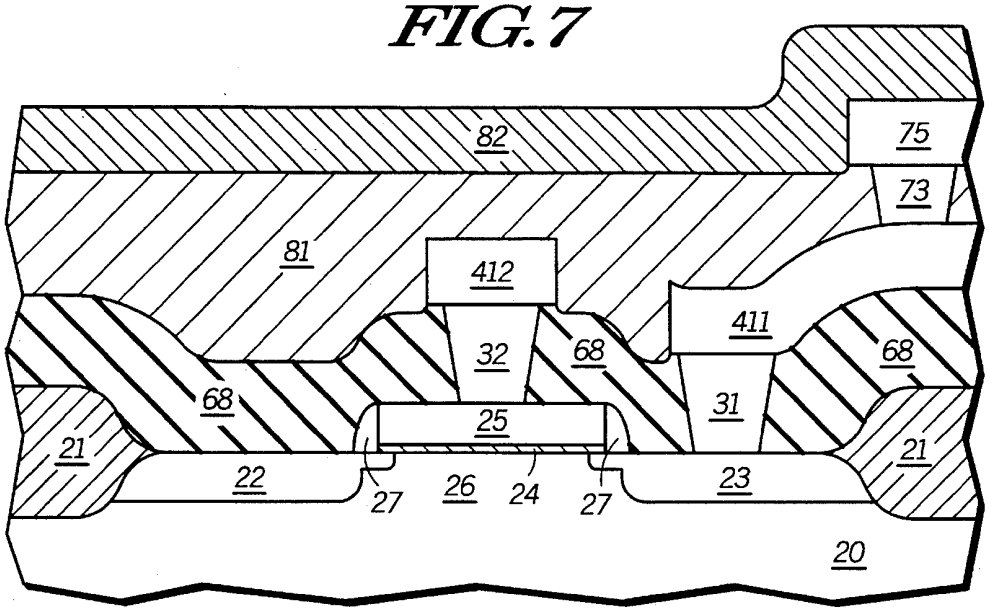

FIG.8

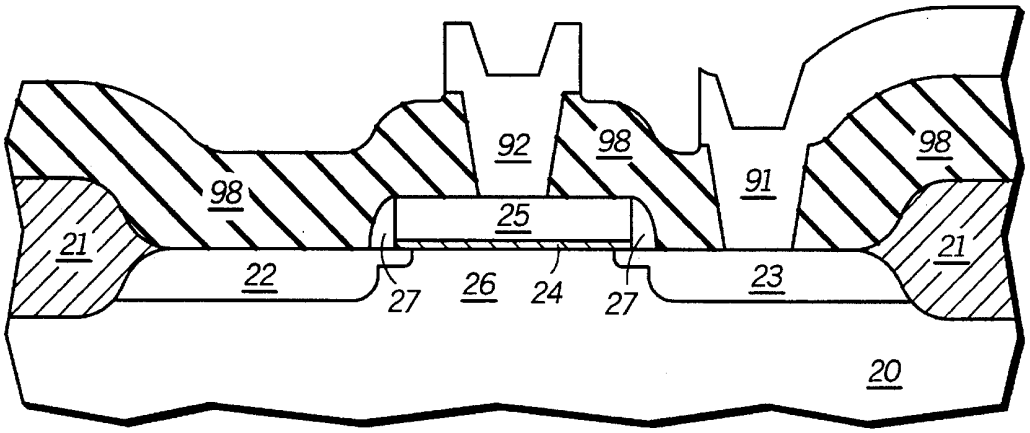

FIG.9

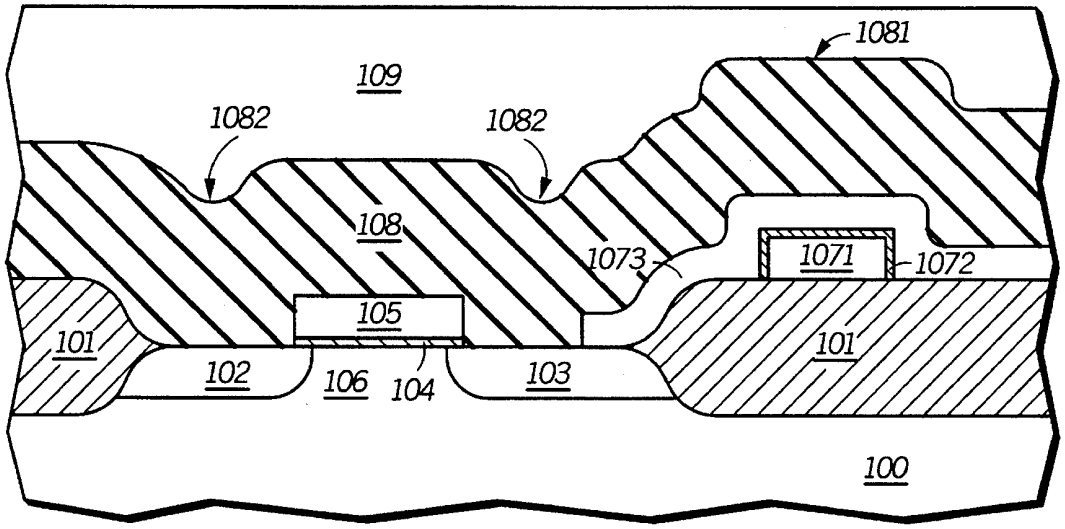

FIG.10

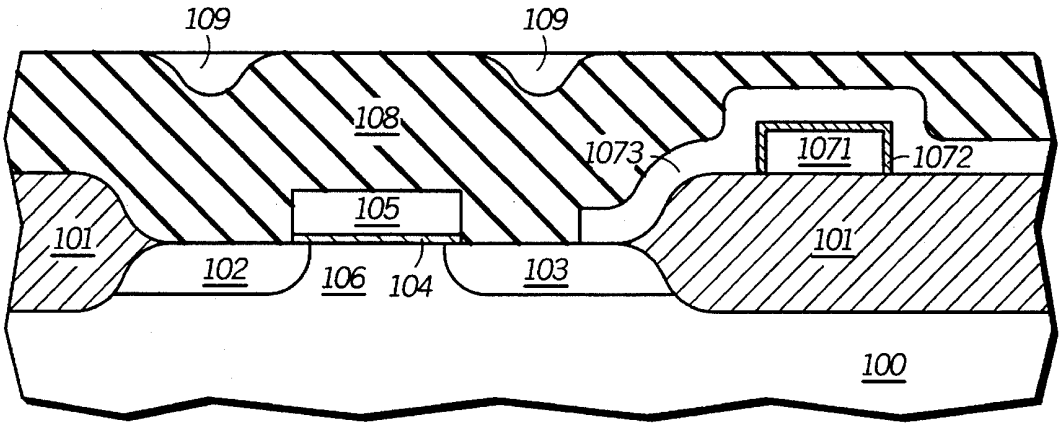

FIG.11

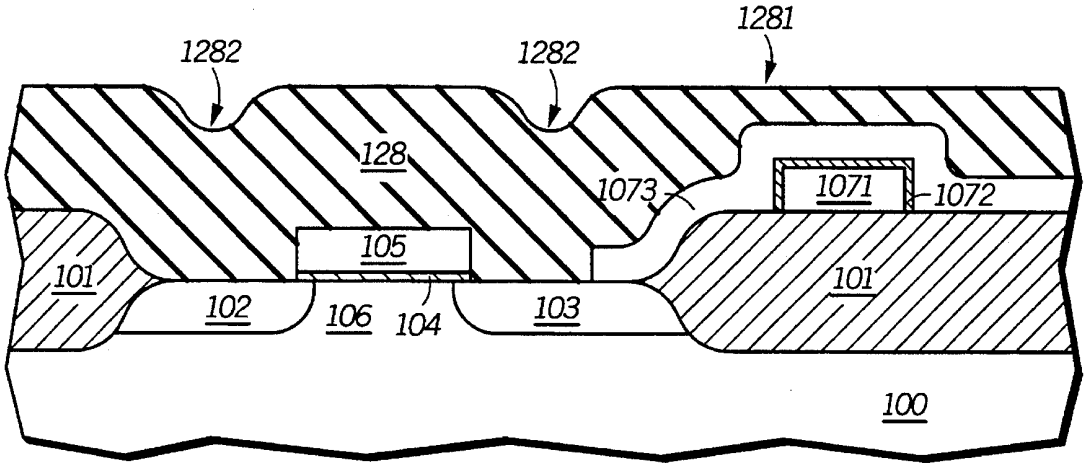
1281
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FIG. 12

PROCESS FOR ETCHING AN INSULATING LAYER AFTER A METAL ETCHING STEP

FIELD OF THE INVENTION

The present invention relates to processes for forming semiconductor devices, and in particular, processes for forming insulating layers and interconnects in semiconductor devices.

BACKGROUND OF THE INVENTION

Interconnects allow various parts of a semiconductor device to be electrically connected with other parts of the semiconductor device. Unfortunately, the processes that form interconnects typically introduce mobile ions that degrade device reliability. Mobile ions, such as sodium, lithium, potassium, calcium, and magnesium, typically come from two sources: during a metal etching step and from an organic solvent typically used in removing a photoresist masking layer. The conventional wisdom of those skilled in the art is that mobile ions introduced during the metal etching steps lie only on exposed surfaces of an insulating layer or an interconnect formed during the metal etching process. A quick deionized water rinse after photoresist removal should remove virtually all of the mobile ions if they lie on exposed surfaces. Semiconductor devices that only have a deionized water rinse after photoresist removal still have unacceptably high device reliability problems.

Organic masking layer solvents include mobile ions. As used in this specification, an organic masking layer solvent is a chemical that is capable of readily removing an organic masking layer (i.e., photoresist, etc.). Examples of organic masking layer solvents include ketones (2-propanone (acetone), etc.), aliphatic hydrocarbons (n-heptane, etc.), alkali-amines (tetramethyl ammonium hydroxide, etc.), and aryl hydrocarbons (toluene, phenol, etc.). Examples of chemicals that are not organic masking layer solvents include alcohols (methanol, ethanol, 2-propanol (isopropyl alcohol), or the like) and glycols (methanediol (methylene glycol), 1,2-ethanediol (ethylene glycol), 1,2-propanediol (propylene glycol), or the like). These latter chemicals typically have at least one hydroxyl group for no more than ten carbon atoms within the molecule, wherein that hydroxyl group is directly attached to a carbon atom other than a carbon atom that is part of an aryl radical (i.e., not phenol). Although the alcohols and/or glycols may attack an organic masking layer, the rate of removing the organic masking layer typically is slow enough that it does not make the alcohols and/or glycols a chemical that readily removes an organic masking layer.

Many photoresist removal processes after a metal etching step use an organic masking layer solvent by itself or an aggregation of plasma ashing and an organic masking layer solvent. Many commercially-available organic solvents have mobile ions concentrations that are measured in parts per million. High-purity organic solvents are available that have mobile ions concentrations as low as about 10 parts per billion. However, these high purity organic solutions may still add mobile ion contamination to semiconductor devices. The cost of the organic solvents increase dramatically with higher purity.

Resist-etch-back processing sequences may also introduce mobile ions into a semiconductor device typically during a plasma etching step. Once again, mobile ions are undesired, and their concentration level in semiconductor devices should be kept as low as possible.

SUMMARY OF THE INVENTION

The present invention includes a process for forming a semiconductor device. The process of the present invention may comprise the steps of: forming a first insulating layer over a semiconductor substrate; depositing a metal-containing layer over the first insulating layer; forming a patterned organic masking layer over the metal-containing layer thereby forming exposed portions of the metal-containing layer; etching the exposed portions of the metal-containing layer with a halide-containing plasma etchant to form an interconnect member; removing the patterned organic masking layer with a plasma gas and not with an organic masking layer solvent; etching a portion of the first insulating layer with a fluoride-containing solution; and forming a second insulating layer over the interconnect member. The step of etching the portion of the first insulating layer etches at least 100 angstroms of the first insulating or removes at least 75 percent of the mobile ions from the first insulating layer. The step of etching the portion of the first insulating layer is performed after the step of etching the exposed portions and prior to forming any layer over the interconnect member; and

The process of the present invention may also comprise the steps of: forming a first insulating layer over a semiconductor substrate, wherein the first insulating layer includes a high point; forming an organic layer over the first insulating layer; simultaneously etching the organic layer and high point; etching a portion of the first insulating layer to a fluoride-containing solution; and rinsing the substrate after the step of etching the portion of the first insulating layer. The step of etching the portion of the first insulating layer etches at least 100 angstroms of the first insulating layer or removes at least 75 percent of the mobile ions from the first insulating layer. The step of etching the portion of the first insulating layer is performed after the step of simultaneously etching and prior to: 1) forming any layer over the first insulating layer; or 2) annealing the substrate including the first insulating layer.

Other features and advantages of the present invention will be apparent from the accompanying drawings and from the detailed description that follows.

BRIEF DESCRIPTION OF THE DRAWINGS

The present invention is illustrated by way of example and not limited to the figures of the accompanying drawing, in which like references indicate similar elements, and in which:

FIG. **1** includes a processing sequence of one embodiment to form a semiconductor device in accordance with the present invention.

FIG. **2** includes a cross-sectional view of a portion of a substrate after forming contact openings.

FIG. **3** includes the substrate of FIG. **2** after forming contact plugs.

FIG. **4** includes the substrate of FIG. **3** after forming an interconnecting level and photoresist members.

FIG. **5** includes the substrate of FIG. **4** after removing the photoresist members.

FIG. **6** includes the substrate of FIG. **5** after etching a portion of a first insulating layer after interconnects have been formed and prior to forming another layer over the first insulating layer and interconnects in accordance with the present invention.

FIG. **7** includes the substrate of FIG. **6** after forming a second insulating layer, a via plug, and an interconnect.

FIG. **8** includes the substrate of FIG. **7** after etching a portion of the second insulating layer and forming passivation in accordance with the present invention.

FIG. **9** includes the substrate of FIG. **2** after forming interconnects and etching a portion of the first insulating layer in accordance with the present invention.

FIG. **10** includes a cross-sectional view of a portion of a substrate prior to a resist-etch-back step.

FIG. **11** includes the substrate of FIG. **10** after etching a portion of an organic layer and a first insulating layer during a resist-etch-back step.

FIG. **12** includes the substrate of FIG. **11** etching a portion of a first insulating layer after the resist-etch-back step in accordance with the present invention.

DETAILED DESCRIPTION OF EMBODIMENTS

Embodiments of the present invention may be used to reduce mobile ion contamination that is introduced into a semiconductor device around the point in processing during steps of a metal etch processing sequence or a resist-etch-back processing step. Mobile ion contamination is believed to be introduced during the plasma metal etching step and during organic masking layer solvent processing for the plasma metal etching step. By eliminating the organic masking layer solvent and etching some of the insulating layer after the plasma metal etching step, mobile ion contamination introduced during the metal etch processing sequence may be substantially reduced. In resist-etch-back processing sequence, mobile ions may be introduced any time an organic layer and insulating layer are simultaneously etched. A portion of the insulating layer is etched to reduce the mobile ion concentration in the insulating layer. The present invention is better understood with the embodiments that are described below.

Interconnect Example

FIG. **1** includes a processing sequence used to form a semiconductor device. The processing sequence includes the steps of: forming contact or via openings **11**; depositing an interconnecting layer **12**; forming a photoresist masking layer **13**; selectively etching the interconnecting layer **14**; removing the photoresist masking layer by ashing (no organic masking layer solvents) **15**; processing the substrate **16**; and depositing an insulating layer **17**.

FIG. **2** includes an illustration of a cross-sectional view of a portion of a semiconductor substrate **20**. Field isolation regions **21**, a source region **22**, and a drain region **23** are formed from a part of the substrate **20** adjacent to its primary surface. The region of the substrate lying between the source and drain regions **22** and **23** and adjacent to the primary surface is a channel region **26**. A gate dielectric layer **24** and a gate electrode **25** overlie the channel region **26** and a portion of the source and drain regions **22** and **23**. Sidewall spacers **27** lie adjacent to the gate dielectric layer **24** and gate electrode **25**, but the spacers **27** are not required. A first interlevel insulating layer **28** including silicon dioxide, borophosphosilicate glass (BPSG), phosphosilicate glass (PSG), or the like overlies the substrate **20** and includes a drain contact opening **291** and a gate contact opening **292**. The first insulating layer **28** is about 8000 angstroms thick, but may be 4000– 20,000 angstroms thick in other embodiments. Conventional steps are used to form the device shown at this point in the process.

A drain contact plug **31** is formed within the drain contact opening **291**, and a gate contact plug **32** is formed within the gate contact opening **292** as shown in FIG. **3**. The contact plugs **31** and **32** may include tungsten; titanium; tantalum; a compound of tungsten, titanium or tantalum; or various combinations of these.

An interconnecting layer **41** and photoresist members **421** and **422** are formed over the first interlevel insulating layer **28** and contact plugs **31** and **32** as shown in FIG. **4**. Exposed portions of the interconnecting layer **41** are formed where the photoresist members **421** and **422** do not overlie the interconnecting layer **41**. The interconnecting layer **41** is a metal-containing layer and includes aluminum, aluminum with silicon, aluminum with copper, aluminum with silicon and copper, copper, or a copper alloy. The interconnecting layer **41** has a thicknesses in a range of 4000–50,000 angstroms. In alternate embodiments, a glue or barrier layer may be part of the interconnecting layer **41** or lie under or over the interconnecting layer **41**. The glue or barrier layer may include titanium nitride, a titanium tungsten, or a titanium-tantalum and have a thickness in a range of 100–3000 angstroms. In addition, an anti-reflecting coating may be a part or overlie the interconnecting layer **41**. The anti-reflecting coating may include a silicon layer, titanium nitride, a titanium-tungsten alloy, or a titanium-tantalum alloy and have a thickness in a range of 50–2000 angstroms. The glue layer, barrier layer, and/or anti-reflective coating (if any of the three are present) would be formed prior to forming the photoresist members **421** and **422**.

The exposed portions of the interconnecting layer **41** (as seen in FIG. **4**) are etched in a plasma reactor during a plasma metal etching step to form the first drain interconnect **411** and the gate interconnect **412** as shown in FIG. **5**. The plasma metal etching step may be performed in a single substrate or batch reactor using reactive ion etching (RIE), or alternately using magnetically enhanced reactive ion etching (MERIE), electron cyclotron resonance (ECR), inductively coupled plasma versions (ICP), or helicon wave (HW) systems. The plasma metal etching step includes a breakthrough or stabilization portion, a main etch portion, an endpoint portion, and an overetch portion. The process may include a chlorine gas, such as molecular chlorine, boron trichloride, carbon tetrachloride, or silicon tetrachloride, any of which may used with or without an accessory gas, such as carbon tetrafluoride, trifluoromethane, nitrogen, helium, or argon. Optionally, bromine-based etchant gases of hydrogen bromide, boron tribromide, or other bromine gases may be substituted for the chlorine gas. During the various portions of the plasma metal etching step, a halide-containing plasma (usually a chlorine-containing plasma) is formed. Ions within the plasma do the actual etching of the exposed portions of the interconnecting layer **41**.

During portions of the plasma metal etching step, typical operating pressures are in a range of 15–40 millitorr (204–544 millipascals), and typical radio-frequency powers are in a range of 750–2500 watts (or alternately expressed in terms of direct-current (dc) volts, in a range of minus 125 to minus 300 volts). The length of the breakthrough portion and the main etch portion are variable due to the thickness and composition of the interconnecting layer **41**. The length of the endpoint portion is sufficient to detect when at least part of the interconnecting layer **41** has been removed over the first interlevel insulating layer **28**.

The overetch portion has a large effect on the implantation of mobile ions into the interlevel insulating layer **28**. This is

due to the interlevel insulating layer **28** being exposed to the ion bombardment of plasma ions and mobile ion contaminants within the plasma. The mobile ion contaminants typically accumulate on the plasma reactor inner surfaces as a result of etching the interconnecting layer **41** and the photoresist members **421** and **422** for this and other previously etched substrates having organic masking layers. These contaminants may become ionized during the plasma metal etching processing sequence. Typical parameters for the overetch portion utilizing batch reactors include pressures no less than 15 millitorr (204 millipascals) and no more than 40 millitorr (544 millipascals), radio-frequency power no less than 1250 watts and no more than 3000 watts, and dc bias no less then 220 volts and no more than 300 volts. The overetch portion length is highly variable. The length may range from 50–500 percent of the length of the endpoint step time, or can be expressed in terms of fixed time ranging from 100–900 seconds. In an alternate embodiment, single substrate reactors for the plasma metal etching step may be used. Other portions of the plasma metal etching step may be performed to prevent metal corrosion after the overetch portion of the plasma metal etching step.

After the plasma metal etching step, the photoresist members **421** and **422** may be removed using at least one conventional plasma ashing technique. The photoresist members **421** and **422** are substantially removed by the plasma ashing step. The photoresist members **421** and **422** are not removed in whole or in part by organic masking layer solvents. FIG. **5** is an illustration at this point in the process.

The first interlevel insulating layer **28** and interconnects **411** and **412** are rinsed with deionized water (optional), exposed to a fluoride-containing etching solution, and rinsed after being exposed to the etching solution. The etching solution typically includes hydrogen fluoride, ammonium fluoride, and a carrier solvent, such as 1,2-ethanediol. Within the etching solution, the hydrogen fluoride is in a range of 0.01–10 weight percent of the solution, ammonium fluoride is in a range of 1.0–50.0 weight percent of the solution, and 1,2-ethanediol makes up the remainder of the solution.

In alternate embodiments, alcohols or other glycols may be used. In general, the alcohols or glycols should have at least one hydroxyl group for every ten carbon atoms within the molecule, wherein that hydroxyl group is directly attached to a carbon atom other than a carbon atom that is part of an aryl radical. Further, the alcohol or glycol should be more viscous than water. The viscosity of the alcohol or glycol at 20 degrees Celsius is typically at least 2 centipoise. 1,2-ethanediol has a viscosity of about 20 centipoise at 20 degrees Celsius. The etching solution and rinsing solution are maintained at a temperature in a range of 20–50 degrees Celsius.

In another alternative embodiment, the hydrogen fluoride may be replaced by additional ammonium fluoride. In other alternate embodiments, the etching solution may include deionized water and/or carboxylic acids (such as acetic acid). The composition of the etching solution may be different when acetic acid is used compared to hydrogen fluoride. In still other embodiments, a surfactant may be included to reduce surface tension and improve the wetting properties of the solution. These wetting agents typically includes a perfluorosurfactant, a linear alkyl sulfonate, or an alkyl benzene sulfonate. For these other embodiments, the content of the components of the etching solution may vary from those previously given.

The solution etching step is designed to etch 100–900 angstroms of the first interlevel insulating layer **28**, and more typically 200–500 angstroms of first interlevel insulating layer **28**. The etching produces a "cleaned" first interlevel insulating layer **68** as shown in FIG. **6**. Various processing factor combinations can be used to form the cleaned first interlevel insulating layer **68**. These combinations are chosen for reasons of equipment stability, process stability, control of the removal rate of the first interlevel insulating layer **28**, or uniformity of the removal rate across the substrate surface. Specific details on the integration of the processing sequence to form the cleaned first interlevel insulating layer **68** may depend upon the equipment for which the processing sequence is integrated. The processing sequence may be performed in an acid hood, an acid-compatible spray tool, or a puddle processing tool. All of these pieces of equipment are known in the art, but the acid-compatible spray tool and the puddle processing tool are briefly described. The acid-compatible spray tool is similar to a spin rinse dryer (SRD) except that the acid-compatible spray tool has been modified to allow the use of acids. The puddle processing tool is a piece of equipment similar to a track used for coating photoresist onto a substrate except that the substrate is sent through at least one "puddle" of a chemical. The substrate is typically spun while it is in the puddle.

The process factors to produce the desired outputs (such as thickness of interlevel insulating layer removal and uniformity) for each equipment type are flexible. For acid hood processing, the exposure time to the etching solution is typically 60–120 seconds. The substrate cassette may or may not be agitated during this time. For the acid-compatible spray or puddle processing tool, the exposure time to the etching solution is typically 45–120 seconds. During the exposure, the substrate cassette or the substrate spin at a speed in a range of 20–75 revolutions per minute. The etching solution is fed into the acid-compatible spray tool or the puddle processing tool at a pressure in a range of 20–50 pounds per square inch (about 138–345 kilopascals) with a flow rate in a range of 0.5–2.5 gallons per minute (about 1.9–9.5 liters per minute). These factors affect the uniformity of the etching and the factors are set within these ranges to adjust for varying substrate sizes and surfaces. The temperature of the etching solution has a large effect on interlevel insulating layer removal rate and is typically 20–30 degrees Celsius.

In one embodiment, the rinsing of the substrate (after the exposure to the etching solution) may include an intermediate solvent rinse and then a deionized water rinse. The intermediate solvent rinse typically includes an alcohol or a glycol that is similar in type to the alcohol or glycol used with the etching solution. An example of the intermediate solvent includes 1,2-ethanediol. The intermediate solvent does not have to be the same solvent used in the etching solution, and therefore, the intermediate solvent may include 2-propanol, 1,2-propanediol, or the like. In alternate embodiments, the intermediate solvent may include deionized water and/or carboxylic acids (such as acetic acid). In still another embodiment, a surfactant may be included to improve the wetting of the intermediate solvent.

The solvent rinse is typically performed at a temperature in a range of 20–90 degrees Celsius. The intermediate solvent rinse time is in a range of 1–10 minutes. For the acid hood, the step may be performed in an overflow tank or quick dump rinser, with or without agitation. For the acid-compatible spray tool or the puddle processing tool, the substrate cassette or the substrate spins at a speed in a range of 25–100 revolutions per minute. For the acid-compatible spray tool or the puddle processing tool, the intermediate

solvent feed pressure and flow rate are typically about the same as the etching solution. The intermediate solvent rinse is followed by a deionized water rinse. The deionized water rinse process spins at a speed in a range of 25–300 revolutions per minute and the feed pressure and flow rate are typically about the same as the etching solution.

In alternate embodiments, additional deionized water rinses may be included. For example, the substrate may be rinsed with deionized water in a quick dump rinser and then be rinsed during a portion of a spin-rinse-dry cycle.

To maximize process integration, the etch using the fluoride-containing solution, intermediate solvent rinse, deionized water rinse, and drying the substrate may be performed sequentially all in as little as one cycle when using an acid-compatible spray tool. This type of process integration reduces cycle time and operator handling.

Further processing forms a second interlevel insulating layer **71**, a via plug **73**, and a second-level interconnect **75** as shown in FIG. **7**. The second interlevel insulating layer **71** may have the same or different composition as the first interlevel insulating layer **28** (as formed). Typically, the second interlevel insulating layer **71** includes an oxide. Although the second interlevel insulating layer **71** is illustrated to be planarized, in alternate embodiments, the second interlevel insulating layer **71** does not need to be planarized. Formation of the via plug **73**, and the second-level interconnect **75** are similar to the formation of the contact plugs **31** and **32** and the interconnects **411** and **412**, respectively.

After the second-level interconnect **75** is formed, the second interlevel insulating layer **71** is processed to form a "cleaned" second interlevel insulating layer **81** as shown in FIG. **8**. The processing to form the "cleaned" second interlevel insulating layer **81** uses a process meeting the criteria as described above with respect to the formation of the cleaned first interlevel insulating layer **68**. Still, the process to form the cleaned second insulating layer may or may not be the same as the process to form the cleaned first interlevel insulating layer **68**. A passivation layer **82**, which is an insulating layer, is formed over the cleaned second interlevel insulating layer **81** and the second-level interconnect **75** to form a substantially finished device as shown in FIG. **8**. Additional insulating layers, via plugs, and interconnecting layers, and other electrical connections may be made, if needed.

FIG. **9** includes an illustration of a cross-sectional view of an alternate embodiment. The alternate embodiment is similar to the one shown in FIG. **5** except that the combination of contact plugs and interconnects are replaced by interconnects **91** and **92**. Therefore, contact plugs are not required. Further processing is performed to form a substantially finished device. Processing with the acid hood, or acid-compatible spray tool, or puddle processing tool is done as described in previous figures to form a cleaned first interlevel insulating layer **98**. Similar to the interconnects **91** and **92**, the via plug **73** and second-level interconnect **75** (shown in FIG. **7**) may be replaced by a single interconnect.

Resist-Etch-Back Example

Some of the mobile ion and other device reliability problems similar to those described in the Interconnect Example may occur with a resist-etch-back process. FIG. **10** includes an illustration of a cross-sectional view of a portion of a semiconductor substrate prior to a resist-etch-back (REB) processing step. Field isolation regions **101**, source region **102**, drain region **103**, and channel region **106** lie at least partially within the substrate **100**. Gate dielectric layer **104** and gate electrode **105** overlie the channel region **106** and portions of the source and drain regions **102** and **103**.

A thin-film transistor overlies one of the field isolation regions **101** and includes a gate electrode **1071**, a gate dielectric layer **1072**, and an active layer **1073**. The active layer **1073** contacts the drain region **103**. A first insulating layer **108** overlies the thin-film transistor and other portions of the substrate **100** and has a composition similar to the first insulating layer **28** described above. The first insulating layer **108** includes high point **1081** and low points **1082**. The difference in elevation between the high point **1081** and low points **1082** may be more than one micron. Such a difference may cause problems with depositions of subsequent layers or lithographic steps. An REB processing sequence is typically performed to reduce the difference. The thin-film transistor may be replaced by another component, such as a metal interconnect or the like. In any event, a difference in elevation between the high and low points **1081** and **1082** of the first insulating layer **108** is too large and needs to be reduced. An organic layer **109**, such as a resist layer, overlies the first insulating layer **108**.

An REB step is performed to remove at least a portion of the organic layer **109** and a portion of the first insulating layer **108** as shown in FIG. **11**. The portion of the REB step in which the organic layer **109** and the first insulating layer **108** are simultaneously etched, has a large effect on the implantation of mobile ions into the first insulating layer **108**. This is due to a similar effect described in relation to overetch portion of the plasma metal etching step as previously described. Typical parameters for the simultaneous etching portion of the REB step when utilizing a batch reactor include pressures no less than 30 millitorr (408 millipascals) and no more than 70 millitorr (952 millipascals), radio-frequency power no less than 800 watts and no more than 1500 watts, and dc bias in a range of minus 350 volts to minus 500 volts, and gas flow ratios of a fluorine-containing gas (such as carbon tetrafluoride, trifluoromethane or the like) and oxygen, no less than one part fluorine-containing gas to one part oxygen and no more than four parts fluorine-containing gas to one part oxygen. The length of the REB step is highly variable. The length may be in a range of 10–60 minutes. The reactor cleanliness has a large effect on mobile ion implantation due to similar effects that were previously described in with respect to the overetch portion of the plasma metal etching step. In an alternate embodiment, a single substrate reactor for the REB step may be used.

The REB etching conditions are chosen, so that the first insulating layer **108** and the organic layer **109** etch at about the same rate. The etching rate of the first insulating layer **108** should be in a range of 0.5–2.0 times the etching rate of the organic layer **109**. During at least a portion of the REB step, both the first insulating layer **108** and organic layer **109** are simultaneously etched. Mobile ions are believed to become implanted into the first insulating layer **108** any time the first insulating layer **108** is exposed during the REB step. After the REB step, portions of the organic layer **109** and insulating layer **108** are present over the substrate **100**. In an alternate embodiment, the thickness of the first insulating layer **108** or REB etching conditions may be changed, so that all of the organic layer **109** is removed, and the first insulating layer **108** is planar. The REB step is performed to make the surface of the first insulating layer **108** more planar and typically does not form openings within the first insulating layer **108** (i.e., not a contact or via etching step).

Any remaining portions of the organic layer **109** are

removed by plasma ashing and without the use of organic masking layer solvents. In an alternate embodiment, the portions of the organic layer **109** may be removed by using organic masking layer solvents by themselves or with the plasma ashing step. The organic masking layer solvents may be used because interconnects or other layers are not exposed.

The first insulating layer is "cleaned" similar to the manner previously described in reference to the first interlevel insulating layer **28** of the Interconnect Example to form a cleaned first insulating layer **128** as shown in FIG. **12** that is similar to the cleaned first interlevel insulating layer **68** as seen in FIG. **6**. The cleaned first insulating layer **128** includes high point **1281** and low points **1282**. In an alternate embodiment, the first insulating layer may be cleaned in a megasonic sink having a dilute fluorine-containing solution, such as 50 parts deionized water to one part hydrofluoric acid, for example. Regardless of the equipment and chemicals used, the amount of the first insulating layer removed to form the cleaned first insulating layer **128** should meet the guidelines described previously with respect to the cleaned first insulating layer **68**.

The difference in elevation between the high and low points **1281** and **1282** is less than the difference in elevation between the high and low points **1081** and **1082** prior to the REB step. The difference is typically less than one micron, and more specifically is in a range of 100–3000 angstroms. The cleaning step of the REB Example is typically performed after the REB step and prior to: forming any other layer over the first insulating layer **108**; annealing the substrate including the first insulating layer **108**; or both.

Benefits

The embodiments of the present invention includes benefits. Mobile ions that are implanted into the insulating layer from the plasma metal etching step may be virtually eliminated by etching the surface of the insulating layer using an etching solution. The etching removes at least 75 percent of the mobile ions from the insulating layers and should remove at least 95 percent of all mobile ions from the insulating layers.

The concentration and depth of the mobile ions within an insulating layer depends on the plasma metal etching parameters that typically depend on the composition and thickness of the interconnecting layer. If any glue or barrier layers, or any anti-reflective coatings are present and etched, the plasma metal etching step may be performed under different parameters than if any of those layers are not present. Different plasma metal etching parameters may affect the concentration and depth of mobile ions within the insulating layer. The cleanliness of the plasma metal etching reactor in terms of mobile ions affects the concentration of same within the insulating layer.

As a result of the plasma etching process, organic masking layers and other polymer films incorporating mobile ions are consumed, releasing mobile ions into the plasma. The mobile ion levels within the reactor continue to increase during successive plasma metal etching cycles, causing higher concentrations of mobile ions to become implanted into an exposed insulating layer, until the interior reactor surfaces are disassembled and cleaned. Due to this accumulation, frequent disassembly and extensive cleaning of the reactor components is required, resulting in lost processing time. The embodiment of the present invention significantly reduces the frequency of cleaning required, and virtually eliminates the need for cleaning solely to reduce mobile ion concentrations within the plasma reactor.

The thickness range of the insulating layer to be removed to achieve the mobile ion reduction levels can be determined by analyzing the insulating layer after the plasma metal etching step is performed, prior to and after solution etching the insulating layer. The analysis can be performed by secondary ion mass spectrometry (SIMS) or equivalent to determine the concentration of mobile ions in the insulating layer. This technique uses an energetic beam of primary ions to sputter away secondary ions from a solid sample. Secondary ions of a given mass to charge ratio may then be plotted as a function of sputtering time. The raw data does not necessarily provide information on the ionic concentration as a function of depth. Due to the energetic effects of SIMS analysis, movement of the ions through the insulating layer occurs and this affects the ions' position during the depth profile, compared to the ions' position prior to the analysis. The total integral of the depth profile does provide mobile ion reduction information by comparison. If known thicknesses of oxide are removed by solution etching the insulating layer prior to SIMS depth profiling, the remaining fraction of the mobile ions can be measured by integration to determine the difference. Etching of oxide thicknesses less than 100 angstroms may result in less than a 75 percent reduction of mobile ions in the insulating layer. Etching of oxide thickness greater than 900 angstroms typically results in no further significant reduction in mobile ion concentration and may cause other problems that are not related to mobile ions. For most mobile ion reduction applications, between 200–500 angstroms of the insulating layer is etched with a fluoride-containing solution after the plasma metal etching step.

Benefits in mobile ion reduction occur with the REB Example, too. Any reduction in mobile ions generally improves device reliability. The amount and depth of mobile ions in the first insulating layer **108** depends on the etching parameters during the REB step. The determination of how much of the first insulating layer **108** is to be etched during the cleaning step may be performed by a SIMS analysis similar to the one described above. Removal of oxide thicknesses less than 100 angstroms may result in less than a 75 percent reduction of mobile ions in the insulating layer. Removal of oxide thickness greater than 900 angstroms typically results in no further significant reduction in mobile ion concentration and may cause other problems that are not related to mobile ions. For most mobile ion reduction applications, between 200–500 angstroms of the insulating layer are solution etched after the REB step.

Another benefit is that organic masking layer solvents are not required. Many of these organic masking layer solvents (particularly alkali-amine solvents) include mobile ions that are present at a concentration of at least 10 parts per billion. Although this is a low concentration, it is large enough to cause device reliability problems. It is believed that the mobile ions present in the solvent may attach to exposed surfaces of the interconnects that may have some residual chlorine, and can attract the mobile ions thereby increasing the mobile ion concentration in the device. High mobile ion concentrations are known to reduce device performance and reliability.

The other advantages of the embodiments of the present invention include virtually complete removal of non-ashable residues and less interconnecting layer damage. Residue removal typically requires exposure to the organic masking layer solvents, such as alkali-amine solvents, to remove these residues. With the exposure to the organic masking

layer solvents, mobile ion additions to the device are almost guaranteed. The etching solution dissolves the residues, as opposed to organic masking layer solvents that break the structures into smaller parts. The etching solution (described in the embodiments above) lowers the adhesion of the residues to the interconnects. Organic masking layer solvents damage interconnects, and the damage may include pitting of the interconnect due to electrolytic dissolution and roughening of the surfaces due to grain removal. Because organic masking layer solvents are not used, the embodiments of the present invention have less damage to the surfaces of the interconnects.

The embodiments of the present invention may require less processing time and less chemicals per cycle compared to organic masking layer solvent processes. The chemicals used in the embodiments described above contain less particles and inherently cause less defectivity. This results in cleaner processing, improved device performance and yield. Separate steps of post-metal etch deionized water rinsing and chemical solution cleaning may be combined into one equipment cycle, reducing processing and staging time, and needed equipment. The use of glycol or alcohol chemicals as a carrier solvent is an advantage due to their higher viscosity than the etchant chemical. This acts as a passivant to protect the interconnect surfaces from excess exposure to the etchant chemical, preventing corrosion and other damage to the interconnects.

In the foregoing specification, the invention has been described with reference to specific embodiments thereof. However, it will be evident that various modifications and changes can be made thereto without departing from the broader spirit or scope of the invention as set forth in the appended claims. Accordingly, the specification and drawings are to be regarded in an illustrative rather than a restrictive sense.

What is claimed is:

1. A process for forming a semiconductor device comprising the steps of:

forming a first insulating layer over a semiconductor substrate;

depositing a metal-containing layer over the first insulating layer;

forming a patterned organic masking layer over the metal-containing layer thereby forming exposed portions of the metal-containing layer;

etching the exposed portions of the metal-containing layer with a halide-containing plasma etchant to form an interconnect member;

removing the patterned organic masking layer with a plasma gas;

etching a portion of the first insulating layer with a fluoride-containing solution, wherein this step:

etches at least 100 angstroms of the first insulating layer; and

is performed after the step of etching the exposed portions and prior to forming any layer over the interconnect member; and

forming a second insulating layer over the interconnect member.

2. The process of claim **1**, wherein the step of etching the portion of the first insulating layer etches at least 75 percent of mobile ions from the first insulating layer.

3. The process of claim **1**, wherein the fluoride-containing solution includes:

hydrogen fluoride;

ammonium fluoride; and

a chemical selected from a group consisting of an alcohol and a glycol.

4. The process of claim **1**, wherein the fluoride-containing solution is at a temperature in a range of 20–50 degrees Celsius.

5. The process of claim **1**, wherein the step of etching the portion of the first insulating layer etches in a range of 200–500 angstroms of the first insulating layer.

6. The process of claim **1**, further comprising a step of rinsing the substrate with deionized water between the steps of etching the exposed portions of the metal-containing layer and etching the portion of the first insulating layer.

7. The process of claim **1**, further comprising steps of:

rinsing the substrate with a chemical selected from a group consisting of an alcohol and a glycol before rinsing the substrate with deionized water;

rinsing the substrate with deionized water; and

drying the substrate,

wherein the steps of rinsing the substrate with a chemical, rinsing the substrate with deionized water, and drying the substrate are performed between the steps of etching the portion of the first insulating layer and forming a second insulating layer.

8. The process of claim **7**, wherein the steps of etching the portion of the first insulating layer, rinsing the substrate with the chemical, rinsing the substrate with deionized water, and drying the substrate are performed in an acid-compatible spray tool during the same cycle.

9. A process for forming a semiconductor device comprising the steps of:

forming a first insulating layer over a semiconductor substrate;

depositing a metal-containing layer over the first insulating layer;

forming a patterned organic masking layer over the metal-containing layer thereby forming exposed portions of the metal-containing layer;

etching the exposed portions of the metal-containing layer with a halide-containing plasma etchant to form an interconnect member;

removing the patterned organic masking layer with a plasma gas;

etching a portion of the first insulating layer with a fluoride-containing solution, wherein this step:

removes at least 75 percent of mobile ions from the first insulating layer; and

is performed after the step of etching the exposed portions and prior to forming any layer over the interconnect member; and

forming a second insulating layer over the interconnect member.

10. The process of claim **9**, wherein the step of etching the portion of the first insulating layer etches in a range of 200–500 angstroms of the first insulating layer.

11. The process of claim **9**, wherein the fluoride-containing solution includes:

hydrogen fluoride;

ammonium fluoride; and

a chemical selected from a group consisting of an alcohol and a glycol.

12. The process of claim **9**, wherein the fluoride-containing solution is at a temperature in a range of 20–50 degrees Celsius.

13. The process of claim 9, further comprising a step of rinsing the substrate with deionized water between the steps of etching the exposed portions of the metal-containing layer and etching the portion of the first insulating layer.

14. The process of claim 9, further comprising steps of:

rinsing the substrate with a chemical selected from a group consisting of an alcohol and a glycol before rinsing the substrate with deionized water;

rinsing the substrate with deionized water; and

drying the substrate,

wherein the steps of rinsing the substrate with a chemical, rinsing the substrate with deionized water, and drying the substrate are performed between the steps of etching the portion of the first insulating layer and forming a second insulating layer.

15. The process of claim 14, wherein the steps of etching the portion of the first insulating layer, rinsing the substrate with the chemical, rinsing the substrate with deionized water, and drying the substrate are performed in an acid-compatible spray tool during the same cycle.

16. The process of claim 1, wherein an organic masking layer solvent is not used to remove the patterned organic masking layer.

17. The process of claim 1, wherein the fluoride-containing solution includes a carrier solvent that has a viscosity of at least 2 centipoise at 20 degrees Celsius.

18. The process of claim 7, wherein:

the fluoride-containing solution includes a carrier solvent; and

each of the carrier solvent and the chemical for rinsing the substrate has a viscosity of at least 2 centipoise at 20 degrees Celsius.

19. The process of claim 9, wherein an organic masking layer solvent is not used to remove the patterned organic masking layer.

20. The process of claim 9, wherein the fluoride-containing solution includes a carrier solvent that has a viscosity of at least 2 centipoise at 20 degrees Celsius.

21. The process of claim 14, wherein:

the fluoride-containing solution includes a carrier solvent; and

each of the carrier solvent and the chemical for rinsing the substrate has a viscosity of at least 2 centipoise at 20 degrees Celsius.

* * * * *

EXHIBIT G

US005776798A

United States Patent [19]

Quan et al.

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[45] Date of Patent: Jul. 7, 1998

[54] **SEMICONDUCTOR PACKAGE AND METHOD THEREOF**

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[52] **U.S. Cl.** **438/112**; 438/460

[58] **Field of Search** 438/112, 113, 438/460, 464, 465

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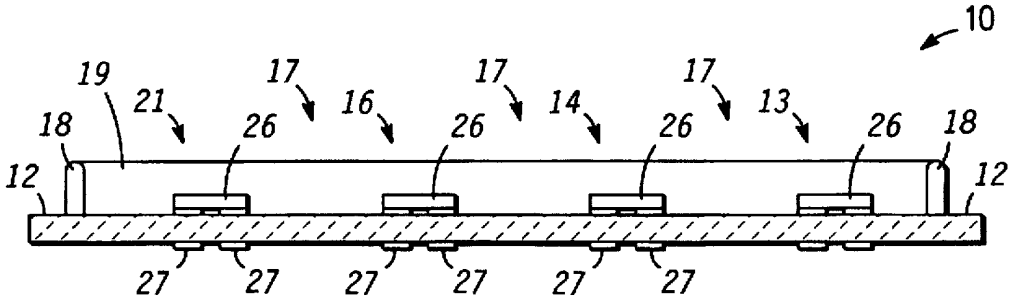
[57] **ABSTRACT**

A semiconductor package substrate (**10**) has an array of package sites (**13**,**14**,**16**,**21**,**22**, and **23**) that are substantially identical. The entire array of package sites (**13**,**14**,**16**,**21**,**22**, and **23**) is covered by an encapsulant (**19**). The individual package sites (**13**,**14**,**16**,**21**,**22**, and **23**) are singulated by sawing through the encapsulant (**19**) and the underlying semiconductor package substrate (**10**).

12 Claims, 1 Drawing Sheet



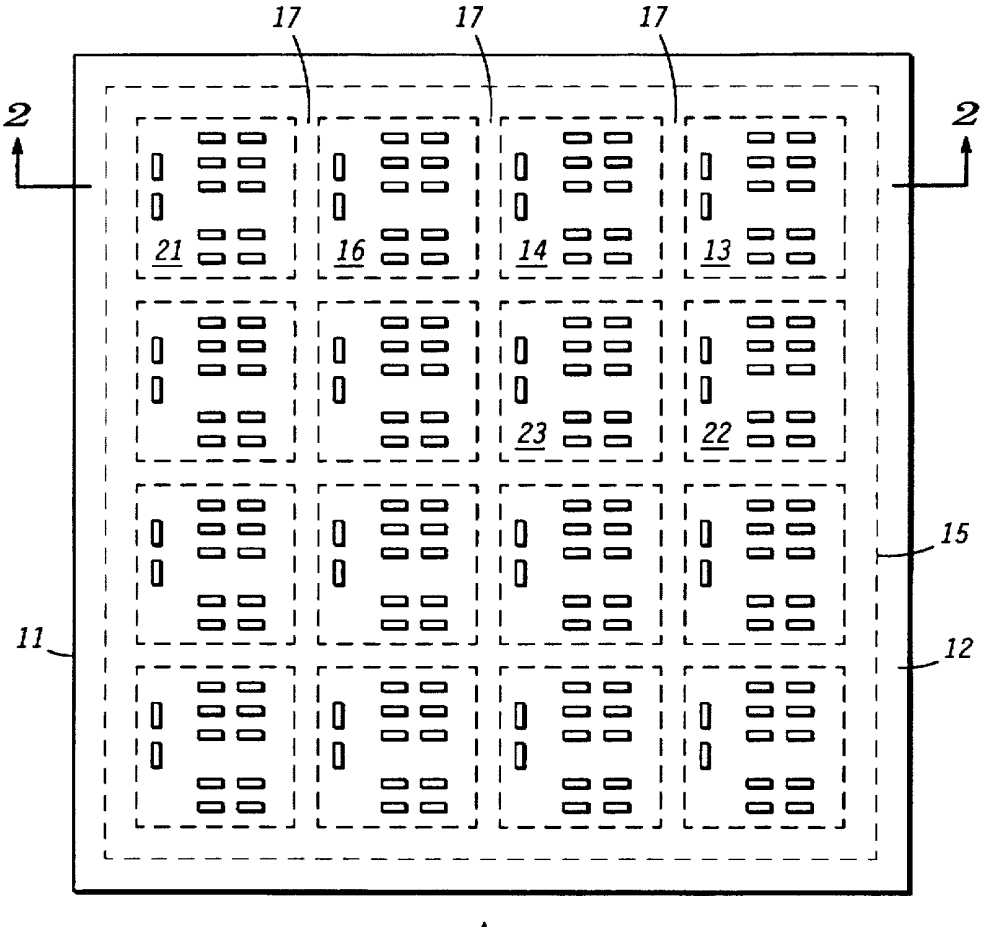


FIG. 1

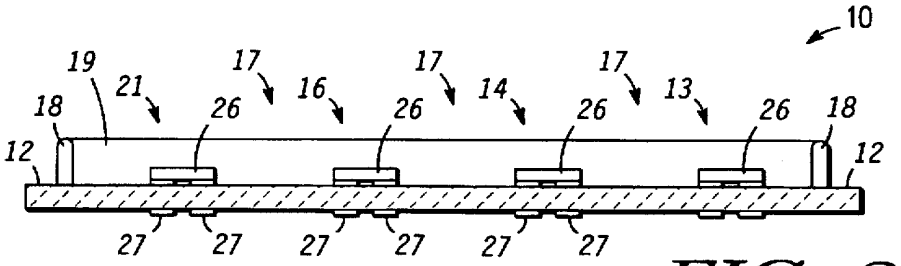


FIG. 2

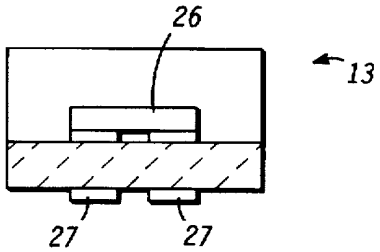


FIG. 3

SEMICONDUCTOR PACKAGE AND METHOD THEREOF

BACKGROUND OF THE INVENTION

The present invention relates, in general, to packaging techniques, and more particularly, to a novel semiconductor package.

In the past, the semiconductor industry has utilized a variety of encapsulation techniques for forming the body of semiconductor packages. Typically, the semiconductor and other devices are assembled onto an interconnect platform or substrate such as a leadframe, printed circuit board or ceramic substrate. One particular encapsulating technique, commonly referred to as glob-top, involves dispensing an encapsulant to cover semiconductor devices or other components that are assembled onto the substrate. One problem with this prior technique is the planarity of the top surface of the encapsulant. Often, the top surface has a convex shape. Because of the convex shape, automated pick and place equipment can not utilize the resulting semiconductor package. Also, it is difficult to mark the top surface because of the convex shape.

Such techniques usually encapsulate a single assembly site on a substrate and after encapsulation, the assembly site is singulated to form an individual package. Consequently, assembly time and singulation time are long and result in high package cost.

Accordingly, it is desirable to have a semiconductor package that has a substantially planar surface that can be utilized with automated pick and place equipment, that is easily marked, and that increases throughput thereby reducing the cycle time and assembly costs.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. **1** illustrates a plan view of a semiconductor package at a stage of manufacturing in accordance with the present invention;

FIG. **2** illustrates a cross-sectional view of the package of FIG. **1** at a subsequent manufacturing stage; and

FIG. **3** illustrates a cross-sectional view of a singulated semiconductor package in accordance with the present invention.

DETAILED DESCRIPTION OF THE DRAWINGS

FIG. **1** schematically illustrates an embodiment of a semiconductor package substrate or semiconductor package **10** at a stage of manufacturing. Package **10** includes an interconnect substrate **11** that has a plurality of package sites such as package sites **13**, **14**, **16**, **21**, **22**, and **23**. As will be seen hereinafter, each of sites **13**, **14**, **16**, **21**, **22**, and **23** will subsequently be singulated into an individual singulated semiconductor package. Each of sites **13**, **14**, **16**, **21**, **22**, and **23** are substantially identical and have areas within each site for attaching and interconnecting a plurality of electronic components such as active semiconductor devices, and passive elements such as resistors and capacitors. Each of sites **13**, **14**, **16**, **21**, **22**, and **23** are separated by a space, for example space **17** between sites **16** and **21**, so that each site may be singulated into an individual package.

Substrate **11** can have a variety of forms including a stamped leadframe, a ceramic substrate, a printed circuit board substrate, and other configurations that are well known to those skilled in the art. As shown in FIG. **1**, substrate **11** is a ceramic substrate having multiple layers of electrical interconnect separated by dielectrics, and multiple attachment areas.

Substrate **11** also includes a dam-bar area **12** around the periphery of substrate **11**, thus, surrounding the periphery of the plurality of package sites as indicated by a dashed line **15**. As will be seen hereinafter, dam-bar area **12** is used for encapsulating package **10** and individual packages formed by each package site of the plurality of package sites, such as sites **13**, **14**, **16**, **21**, **22**, and **23**.

FIG. **2** illustrates a cross-sectional schematic of package **10** at a subsequent stage of manufacturing and is taken along cross-sectional line **2**—**2** shown in FIG. **1**. The same reference numbers are used to represent the same elements among the drawings. Typically, components such as semiconductor devices or passive elements are attached to each package site as illustrated by a component **26** attached to sites **13**, **14**, **16**, and **21**. Many components may be attached to each package site, device **26** is shown only for illustration purposes. As shown in FIG. **2**, encapsulating each package site of the plurality of package sites and associated components includes forming a dam-bar **18** on area **12**. Dam-bar **18** creates a cavity containing the plurality of package sites. Dam-bar **18** is formed by dispensing a first encapsulating material onto area **12**. The first encapsulating material has a first viscosity that is sufficiently high so that the encapsulating material does not flow across substrate **11** but substantially remains as dispensed onto area **12**. Typically, the first encapsulating material has a high viscosity that is greater than approximately 500,000 centi-poise (cps), and typically has a viscosity of 1,000,000 to 2,000,000 cps at approximately 25° C. (degrees Celsius). One suitable first encapsulating material for dam-bar **18** is a rigid thermosetting epoxy such as FP-4451 manufactured by Hysol-Dexter of Industry, Calif.

Generally, the first encapsulating material is heated during dispensing by heating the syringe or dispensing mechanism so that the first encapsulating material can be dispensed. Additionally, substrate **11** generally is also heated to a higher temperature so that the first encapsulating material flows sufficiently to form dam-bar **18**. Generally, the dispensing mechanism or syringe is heated to approximately forty to fifty degrees Celsius (40°–50° C.), and substrate **11** generally is heated to approximately eighty to ninety degrees Celsius.

Thereafter, a second encapsulating material is dispensed within the cavity formed by dam-bar **18** to form an encapsulant **19** covering the components on substrate **11**. The thickness of encapsulant **19** is sufficient to cover and protect components such as component **26** formed on substrate **11**. The second encapsulating material has a second viscosity that is sufficiently low so that the second encapsulating material flows to fill the cavity leaving no voids and surrounds the components and attachment wires used to connect components to substrate **11**. The second viscosity is less than the 500,000 cps high viscosity of the first encapsulating material and typically is approximately 20,000 to 200,000 cps at 25° C. One example of a suitable material for the second encapsulating material is FP-4650 manufactured by Hysol-Dexter. Additionally, the second encapsulating material typically has the same chemical base as the first encapsulating material so that the two materials bond at the interface to minimize separation and potential contamination. During dispensing, the second encapsulating material and substrate **11** are heated similarly to the heating used for dispensing the first encapsulating material.

After dispensing, the first and second encapsulating material are heated to gel both encapsulating materials in order to control subsequent out gassing and warpage of substrate **11**. Typically, both encapsulating materials are gelled for

approximately one hour at one hundred ten degrees Celsius. Subsequently, dam-bar **18** and encapsulant **19** are cured so that encapsulant **19** forms a continuous encapsulating material covering the underlying components. Typically the curing is performed at a temperature of approximately 165° C. for a time of up to two hours. After curing, each individual package site is singulated into a singulated package by using space **17** for sawing completely through encapsulant **19** and substrate **11**. For example, a ceramic saw is used to saw through encapsulant **19** and substrate **11** when substrate **11** is ceramic material. Other singulation techniques could be utilized including laser cutting through encapsulant **19** and substrate **11**.

The area covered by encapsulant **19** should be larger than the meniscus formed by the second encapsulating material so that the top surface of encapsulant **19** remains substantially planar. For example, the top surface should have a deviation of less than plus or minus 0.13 millimeters across the surface of encapsulant **19**. As shown in FIG. **2**, the plurality of package sites are formed in an 4×4 array but could also be formed in other arrays. An array that is sixty by sixty millimeters provides a sufficient area to provide the desired planarity.

It should be noted that other encapsulating techniques could be utilized to cover the plurality of package sites with an encapsulating material in order to encapsulate package **10**. For example, dam-bar **18** could be a premanufactured frame applied to area **12**, and overmolding or other techniques could be used for the encapsulating. Thereafter each package site can be singulated as described hereinbefore.

FIG. **3** illustrates a cross-sectional view of a singulated package formed from a package site such as package site **13** shown in FIG. **1** and FIG. **2**.

By now it should be appreciated that there has been provided a novel semiconductor package and method therefor. Forming a plurality of package sites on a substrate and using one dam-bar around the entire periphery surrounding the plurality of package sites, facilitates forming a substantially planar surface on the encapsulant. Forming a substantially planar surface allows each singulated package to have a substantially planar surface and facilitates utilization with automated pick and place equipment, and also facilitates clear marking of each singulated package. Forming the plurality of package sites adjacent to each other and covering the plurality of package sites with one continuous encapsulant minimizes space required to singulate the package sites and maximizes the number of package sites on a substrate thereby providing the smallest package outline and lowering package costs.

We claim:

1. A method of forming a semiconductor package comprising:

forming a substrate having a plurality of package sites and an electronic component attached to the plurality of package sites;

encapsulating the plurality of package sites wherein the encapsulating forms a continuous encapsulating material covering the plurality of package sites; and

singulating through the encapsulating material to singulate each package site into an individual package.

2. A method of forming a semiconductor package comprising:

encapsulating a plurality of package sites that are on a substrate wherein the encapsulating forms a continuous encapsulating material covering the plurality of package sites and wherein encapsulating the plurality of package sites includes forming the encapsulating material to have a top surface planarity deviation of less than 0.13 millimeters; and

singulate through the encapsulating material to singulate each package site.

3. A method of forming a semiconductor package comprising:

encapsulating a plurality of package sites that are on a substrate wherein the encapsulating forms a continuous encapsulating material covering the plurality of package sites and wherein encapsulating the plurality of package sites includes forming a dam bar surrounding the periphery of the plurality of package sites for forming a cavity containing the plurality of package sites, and dispensing the encapsulating material within the cavity; and

singulating through the encapsulating material to singulate each package site.

4. The method of claim **3** wherein forming the dam bar includes dispensing a first encapsulating material having a first viscosity.

5. The method of claim **4** wherein dispensing the encapsulating material within the cavity includes dispensing a second encapsulating material having a second viscosity that is lower than the first viscosity.

6. The method of claim **5** wherein dispensing the first encapsulating material having the first viscosity includes having a viscosity of 1,000,000 to 2,000,000 cps.

7. The method of claim **5** wherein dispensing the second encapsulating material having the second viscosity includes having a viscosity less than 500,000 cps.

8. The method of claim **5** further including gelling both the first and second encapsulating materials prior to curing both the first and second encapsulating materials.

9. The method of claim **5** wherein dispensing the first encapsulating material includes heating the first encapsulating material.

10. The method of claim **5** wherein dispensing the second encapsulating material includes heating the second encapsulating material.

11. The method of claim **1** wherein singulating through the encapsulating material includes sawing through the encapsulating material and the substrate.

12. The method of claim **1** wherein encapsulating the plurality of package sites includes encapsulating by overmolding.

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UNITED STATES PATENT AND TRADEMARK OFFICE

CERTIFICATE OF CORRECTION

PATENT NO. : 5,776,798

DATED : July 7, 1998

INVENTOR(S) : Son Quan et al.

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

In column 4, claim 2, line 13, delete "singulate" and insert –singulating--.

Signed and Sealed this

Fifteenth Day of June, 1999

Attest:

Q. TODD DICKINSON

Attesting Officer

Acting Commissioner of Patents and Trademarks